Compact MOS Modelling for RF CMOS Circuit Simulation

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Abstract

Modern CMOS technologies are becoming increasingly attractive for RF applications. This imposes stringent requirements on compact models used in circuit simulation: not only currents and charges, but also noise, power gain, impedances, and harmonic distortion must be modelled accurately. In this paper several of these issues will be addressed with the help of Philips' new public-domain compact MOS model, MOS Model 11.

1 Introduction

As modern CMOS is rapidly progressing towards sub-100 nm dimensions, RF performance of MOS devices is improving strongly [1, 2, 3]. As a consequence, CMOS has become a viable option for RF applications. In order to exploit the RF capabilities of CMOS, compact models for circuit simulation are required that describe all the relevant quantities the RF designer is interested in: not only currents and charges, but also noise figure, power gain, impedance levels, and harmonic distortion [4, 5, 6].

In this paper, several of these issues will be addressed with the help of Philips' new compact MOS model, MOS Model 11. This model gives a good description of the currents and all its derivatives up to the 3rd order, enabling accurate distortion modelling (see Section 2). Using this model, we show that thermal noise can be described very well without the need of any additional parameters (see Section 3). Next, we show how non-quasi-static effects can be modelled using the concept of channel segmentation (see Section 4).

2 RF Distortion

The compact MOS Model named 'MOS Model 11' (MM11) [7], the successor of MOS Model 9, has been developed in order to accurately describe the MOSFET currents themselves as well as their higher-order derivatives (up to 3rd order) with respect to all terminal voltages. The model is based on a continuous description of the surface potential throughout all operating regimes, including the increasingly important moderate inversion regime. Compared to contemporary models such as BSIM4 [8] and MOS Model 9 [7], the new model contains improved expressions for mobility reduction and velocity saturation. All relevant physical effects in today's MOSFETs, such as

poly depletion, bias-dependent overlap capacitances, quantum-mechanical effects, and gate leakage current are included. In this section we will show that the model gives an excellent description of harmonic distortion, both at low and RF frequencies.

2.1 Experimental method

As illustrated in Fig. 1, a sinusoidal gate voltage leads to a distorted drain current, containing the ground harmonic (HD1) as well as unwanted higher-order harmonics (HD2, HD3...). This has been measured from 16 MHz to 1 GHz using an RF network analyzer (HP8753E) with an extension to measure the 2nd and 3rd harmonic power levels [9]. Measurements are de-embedded up to the test-structure terminals [9]. Compact model parameters for MM11 are extracted from the DC current and its 1st-order derivatives, and from low-frequency CV measurements. The compact model has been extended with parasitic resistances to describe polysilicon [10, 11] and bulk resistance [12] effects.

2.2 Results

Measured and modelled results for a 0.35 μm n-MOS transistor as a function of DC gate bias are shown in Fig. 2 for an intermediate frequency (f=16 MHz), and in Fig. 3 for an RF frequency (f=1 GHz). RF results for an 0.18 μm n-MOS transistor in 0.18 μm technology are shown in Fig. 4. In all cases it is observed that MM11 (solid lines) gives an accurate description of HD1, HD2, and HD3. Simulations of HD3 using BSIM3v3 and MOS Model 9 are also shown for reference. In contrast to what has been observed for bipolars [14], it was found that at f=1 GHz the description of distortion is still mainly determined by the drain current model of the MOSFET, while the parasitic and intrinsic charges only contribute about -57 dBm to HD3. Accurate modelling results have also been obtained for different values of drain bias, different technologies, and for PMOS, see for instance Ref. [13].

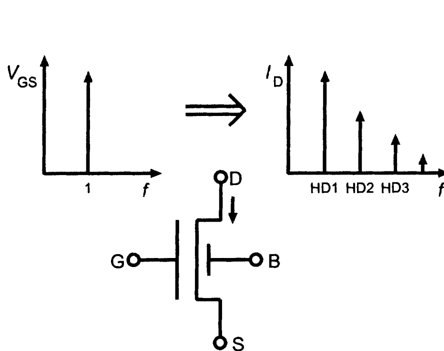

Fig. 1: A sinusoidal V_{GS} results in a distorted drain current I_D containing not only the ground harmonic (HD1) but also unwanted higher-order harmonics (HD2, HD3...), due to the non-linear dependence of I_D on V_{GS}.

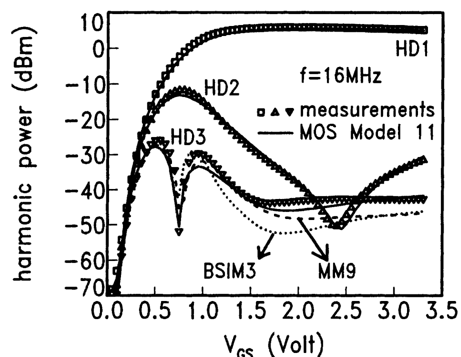

Fig. 2: LF distortion (f = 16 MHz) as a function of V_{GS} of a 16 × 10/0.35 μm n-channel device in 0.35 μm technology. V_{DS} = 3.3 V; P_{in} = −5 dBm.

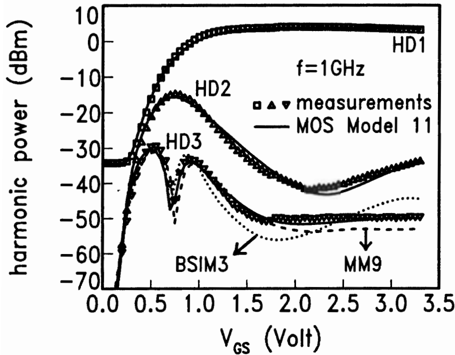

Fig. 3: RF distortion (f = 1 GHz) as a function of V_{GS} on the same device as in Fig. 2, i.e. a 16 × 10/0.35 μm n-channel device in 0.35 μm technology. V_{DS} = 3.3 V; P_{in} = −5 dBm.

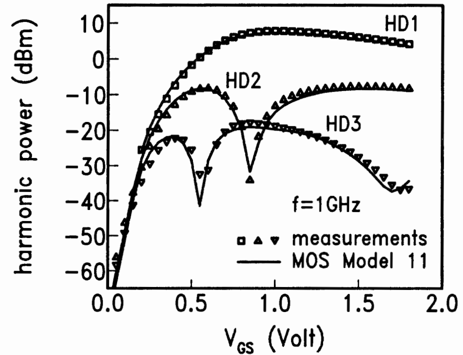

Fig. 4: RF distortion (f = 1 GHz) for a 64 × 3/0.18 μm n-channel device in 0.18 μm technology. V_{DS} = 1.8 V; P_{in} = −5 dBm.

3 Thermal noise

Accurate modelling of thermal noise is a prerequisite for the application of modern CMOS technologies to low-noise RF circuit design. In some publications [15, 16], it has been reported that the thermal noise in submicron MOSFETs is increased considerably w.r.t. the predictions based on long-channel thermal noise theory. The reported enhancements amount to more than a factor of 10 for n-channel devices as long as 0.7 μm, and are often attributed to hot-carrier effects. Contrary to this, we will show that the drain current thermal noise of deep-submicron MOSFETs can be described accurately *without* invoking carrier heating or introducing any parameters (see also Ref. [17]). This is achieved by using the Klaassen-Prins formula [18, 19] combined with the appropriate equations for velocity saturation [17]. For the resulting expressions we refer to [7].

3.1 Experimental method

Drain current thermal noise is investigated at an intermediate frequency (248 MHz) where both low-frequency 1/f noise, and high-frequency induced gate noise can be neglected. We study the 50-Ohm noise figure F_{50} (i.e. the noise figure at 50 Ω generator impedance), which is dominated by the MOSFET drain current thermal noise. The on-wafer noise measurements are performed using a conventional noise figure test set. A 50-Ω resistor is used to match the output impedance to the noise figure meter input. Besides the noise measurements, standard DC-characterization has been performed in order to determine the compact model parameters for each device. Besides the noise contribution of the MOSFET itself, all the device and interconnect parasitics, RF-probes, cables and bias-tees and the 50-Ω matching resistor have been characterized experimentally and included in the simulations.

3.2 Results

In Figs. 5 and 6 F_{50} is plotted as a function of V_{GS} for a number of channel lengths in 0.35 μm technology. It is seen that the thermal noise model, as described above, gives an excellent fit to the data. The same conclusion is drawn from Figs. 7 and 8, where F_{50} is plotted as a function of V_{GS} and V_{DS}, respectively, for a 0.18 μm device in a 0.18 μm technology. Note that all parameters used in the noise model are obtained from DC and CV measurements; all our experimental results are described accurately *without* introducing additional noise parameters, or invoking carrier heating or new physical phenomena. Of course we do not deny the existence of the physical effect of carrier heating; we simply find that the effect is not large enough to enhance the thermal noise to a measurable extent. The interesting question remains of course why Refs. [15, 16] *do* find such a large enhancement. Possibilities are (i) noise of the weak avalanche current [20] (ii) noise due to bulk resistance (included in our model) [21] or (iii) a generation-recombination noise contribution.

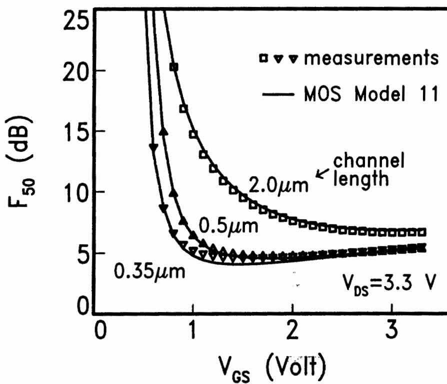

Fig. 5: F_{50} as a function of V_{GS} for n-channels in 0.35 μm technology. Gate lengths are 2 μm, 0.5 μm, 0.35 μm, gate width is 16 × 10μm.

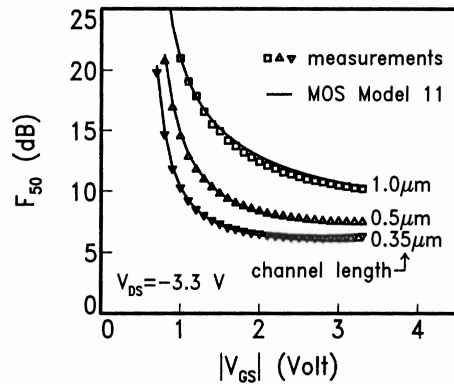

Fig. 6: F_{50} as a function of V_{GS} for p-channels in 0.35 μm technology. Gate lengths are 2 μm, 0.5 μm, 0.35 μm, gate width is 16 × 10μm.

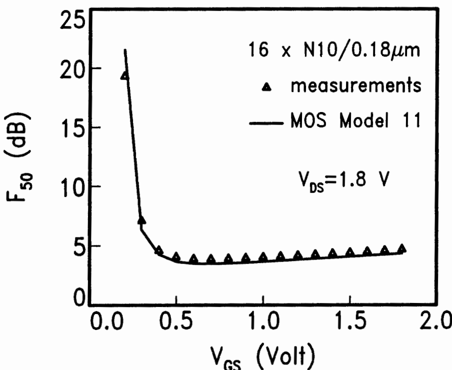

Fig. 7: F_{50} as a function of V_{GS} for 16 × 10/0.18 μm n-channel in 0.18 μm technology.

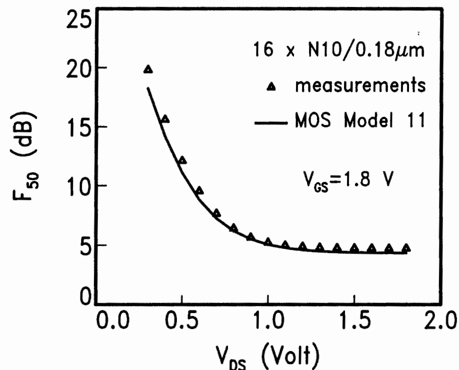

Fig. 8: F_{50} as a function of V_{DS} for 16 × 10/0.18 μm n-channel in 0.18 μm technology.

4 Non-quasi-static effects

To facilitate RF CMOS circuit design, RF modelling tools should give an accurate description of quantities like power gain, input impedance and the phase delay between drain current and gate voltage. To achieve this, not only parasitic resistances [10, 12], but also effects of finite channel transit times have to be taken into account. These so-called non-quasi-static (NQS) effects are included in various small-signal models (see e.g. [19, 22, 23]), which are, however, not suited for large-signal, transient and harmonic-balance simulations. An alternative model is the NQS extension of BSIM3 [24], which is computationally efficient, but is restricted to large-signal analysis. We follow the approach illustrated in Fig. 9, which is based on the idea of channel segmentation [19, 25, 26]. Advantages of this approach are that (i) it is physically sound, (ii) it can be used in all kinds of circuit analysis (DC, small-signal, transient, and noise analysis), and that (iii) all parameters are determined from DC- and low-frequency CV-measurements.

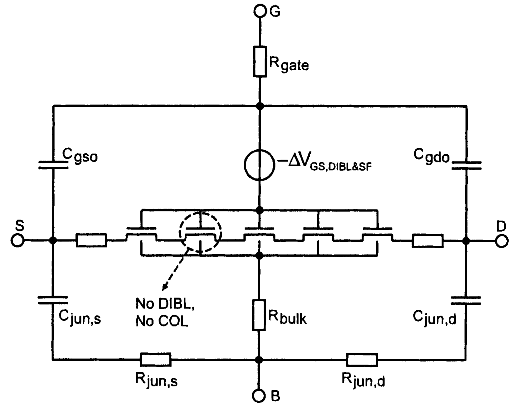

Fig. 9: NQS model consisting of five MM11 segments.

4.1 Experimental method

Using an HP8510 network analyzer, small-signal S-parameters [27] have been measured on a number of devices in ground-signal-ground configuration, fabricated in an 0.18 μm CMOS technology. The measured S-parameters are converted into Y-parameters [27] and de-embedded up to the test-structure terminals. From the Y-parameters, relevant quantities such as input impedance and maximum stable/available power gain are calculated.

4.2 Input resistance

One of the key parameters for the RF CMOS designer is the input impedance. Here we consider the input impedance in case the output is ac-shortcircuited, which is given by $R_{\text{in}} = \text{Re}(1/Y_{11})$. This quantity is of special interest since it is equal to zero for a QS model without parasitic resistances. In reality, however, it has a finite value (see Fig. 10), which is partly due to parasitic resistances, but mainly due to the NQS effect. This is shown in Fig. 10 by varying the number of channel segments in our NQS model: by increasing the number of segments, the modelled curve rapidly approaches the measurements. In the linear regime of operation, it can be shown analytically that for frequencies well below f_{T}:

$$R_{\text{in}}(N_{\text{seg}}) = R_{\text{in}}^{\text{NQS}} \cdot \left(1 - \frac{1}{N_{\text{seg}}^2}\right) \tag{1}$$

where $R_{\text{in}}^{\text{NQS}}$ is the full NQS input impedance ($N_{\text{seg}} = \infty$). We have found empirically that Eq. (1) holds also for the saturation mode. From Eq. (1) we see that, using 5 segments, the modelled R_{in} only deviates 4% from $R_{\text{in}}^{\text{NQS}}$. Using 5 segments an accurate description is also obtained for R_{in} as a function of V_{GS} for a number of channel lengths (see Fig. 11).

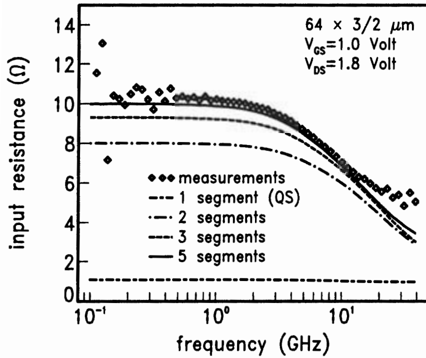

Fig. 10: Symbols: input resistance versus frequency for a 64 × 3/2 μm n-channel in 0.18 μm technology. Lines are calculated with different number of channel segments.

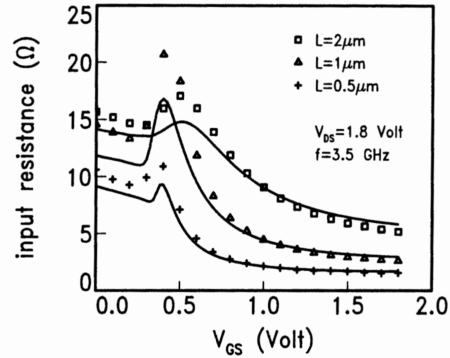

Fig. 11: Symbols: input resistance at 3.5 GHz versus V_{GS} for a number of channel lengths. Gate width is 64×3 μm. Lines are calculated with a 5-segment NQS model.

4.3 Maximum power gain

Another quantity of interest is the maximum stable/available power gain [27], which we define as:

$$G_{\text{msg/max}} = \begin{cases} |\frac{Y_{21}}{Y_{12}}| & \text{if } K < 1 \\ |\frac{Y_{21}}{Y_{12}}| \cdot \left(K - \sqrt{K^2 - 1}\right) & \text{otherwise} \end{cases} \tag{2}$$

where K is the Rollett stability factor, given by

$$K = \frac{2\text{Re}(Y_{11})\text{Re}(Y_{22}) - \text{Re}(Y_{21}Y_{12}))}{|Y_{21}Y_{12}|} \tag{3}$$

The frequency at which $G_{\text{msg/max}} = 1$ defines the maximum oscillation frequency f_{max}. In Fig. 12, it is seen that a quasi-static model is not able to predict f_{max} for an $L = 2$ μm device. Using the NQS model, however, it is seen that the fit between model and data improves considerably when the number of segments is raised to five. In general, the number of segments needed depends on the channel length and the operation frequency. Using 5 segments only, we see in Fig. 13 that G_{max} is modelled very well for a range of channel lengths $L < 2$ μm over the full gate bias range in saturation.

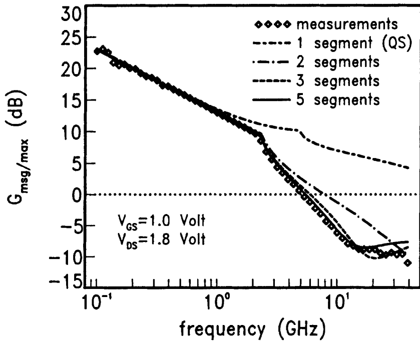

Fig. 12: Symbols: maximum stable/available power gain versus frequency for a 64 × 3/2 μm n-channel in 0.18 μm technology. Lines are calculated with different number of channel segments.

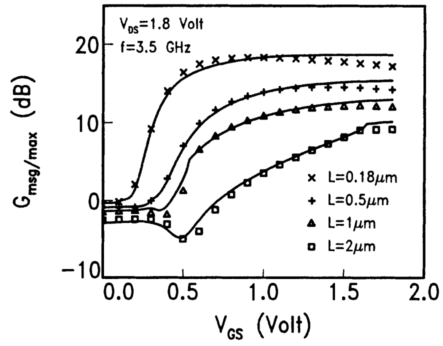

Fig. 13: Symbols: maximum stable/available power gain at 3.5 GHz versus $V_{\rm GS}$ for a number of channel lengths. Gate width is 64 × 3 μm. Lines are calculated with a 5-segment NQS model based on MM11.

4.4 High-frequency distortion and non-quasi-static effects

Finally we discuss the impact of NQS effects on RF distortion. In Fig. 14, 1 GHz distortion data for a 2μm n-channel transistor are shown. At low values of gate bias the QS model no longer gives good results. In this bias region the harmonic frequency exceeds the cut-off frequency $f_{\rm T}$ and as a result the quasi-static approach is no longer valid. Fig. 15 shows that the NQS-model with N=10 segments gives accurate results over almost the whole bias region.

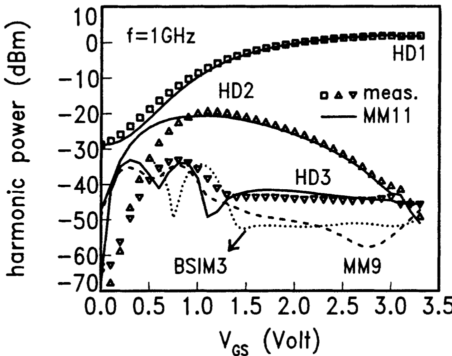

Fig. 14: First, second, and third harmonic distortion power levels of a W/L = 160/2 μm n-channel device in 0.35 μm technology. $V_{\rm DS}$ = 3.3 V; $P_{\rm in}$ = −5 dBm.

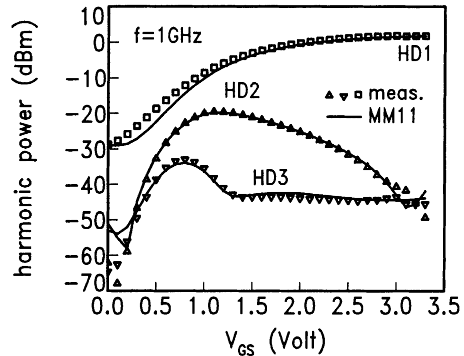

Fig. 15: Same measurements as in Fig. 14. Solid line is calculated with a 10-segment NQS model based on MM11.

5 Conclusion

In this paper, various aspects of compact modelling for RF CMOS have been addressed. First, we have shown that MOS Model 11 forms an excellent basis for RF CMOS circuit design, because, in contrast to other contemporary compact models, it is able to describe accurately the higher-order derivatives of the drain current, which results in an excellent description of third-order harmonic distortion. Moreover, we have shown that drain current thermal noise can be *predicted* with MOS Model 11: carrier heating effects or other additional physical effects do not need to be included to get a good description of the noise data. Finally, we have presented a simple yet effective method to turn a QS model into an NQS model by applying channel segmentation.

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