Differences Between Quantum-Mechanical Capacitance-Voltage Simulators*

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Abstract

We present an extensive benchmarking comparison of an ensemble of the most advanced quantum-mechanical (QM) capacitance-voltage (CV) simulators available. Quantitative differences in the accumulation capacitance of p-channel and n-channel devices as large as 20% are found in a systematic comparison. Some of the underlying physics and models that lead to the observed differences are described.

1 Introduction

Increasingly complex and sophisticated methods to simulate CV curves are needed to describe the additional physics (such as QM quantization and poly-Si depletion) associated with ultrathin gate dielectrics which make it difficult to predict MOS CV curves accurately[1-8,10]. Recently, we showed for n-channel (p-substrate) capacitors, that an ensemble of advanced QM simulators have similar performance accounting for polysilicon depletion and QM confinement; however, there are quantitative differences of up to 20% in the accumulation capacitance for ultrathin gate dielectric devices[1]. These differences indicate that parameters extracted from experimental CV curves (such as the effective oxide thickness, EOT[1]) are dependent upon the analysis software; therefore, it is critical that the inter-relationship of the simulators be well-characterized. This paper presents, for the first time, a systematic comparison of QM simulators for p-channel (n-substrate) devices, and it discusses and illustrates some of the underlying physical and modeling differences that lead to observed discrepancies between simulators. A method to extend the comparison to include 2D simulators is also discussed.

2 Simulator Ensemble

Six of the most advanced, one-dimensional, QM CV software packages were compared in this study: (1) the Quantum Mechanical CV Simulator[2] from the Device Group at UC-Berkeley (Berkeley), (2) NEMO, the Nanotechnology Engineering Modeling Program[3], (3) CVC[4], by Hauser at NCSU (NCSU), (4) UTQuant[5], from UT-Austin, (5) SCHRED[6], from an Arizona State/Purdue team, and

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(6) IBM's Tqm_v6[7]. In addition, we have developed in-house CV code[8] that is used to gain insights into how different physical approximations affect CV simulation results. Three of these simulators (Berkeley, UTQuant, and SCHRED) are based upon self-consistently solving the Schrödinger and Poisson equations. NEMO is a non-equilibrium Green's function solver, while NCSU and the in-house code are based upon models containing physics approximations enabling rapid calculation. IBM's Tqm_v6 is a QM CV analysis program based upon the results of IBM's extensive QM simulations. Simple n-channel and p-channel poly-Si gated MOS capacitor test structures were used to compare the various simulators.

3 Results and Discussion

A matrix of CV curves was created for comparison by varying the parameters (substrate doping, N_d, poly-Si doping, N_{poly}, and ideal SiO_2 thickness, d_{ox}). Figure 1 shows typical CV simulations for p-channel capacitors with $d_{ox} = 2.0$ nm[9]. Similar results are obtained for the n-channel devices. Figure 1 illustrates that the overall shape of the CV curves is the same; i.e., the simulators are qualitatively similar. However, there are important differences between the simulators. The largest difference is in the accumulation region capacitance, which leads to CV curves that appear to be from devices having different d_{ox}.

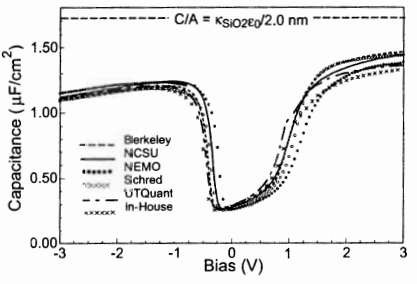

Figure 1: p-channel CV curves including QM confinement and poly-Si depletion. d_{ox} = 2.0 nm (1.901 nm for NEMO), N_d = 1 x 10^{18} cm^{-3}, and N_{poly} = 1 x 10^{20} cm^{-3}.

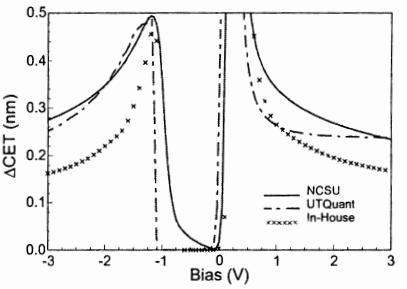

Figure 2: ΔCET for three different simulators. n-channel, d_{ox} = 2.0 nm, Nd = 1 x 10^{18} cm^{-3}.

We have used Tqm_v6, IBM's QM CV analysis program, to extract a reduced set of thickness parameters (or assessment criteria) for each simulated CV curve as a quantitative method to compare the results of the various simulators. Table 1 shows the extracted EOT and capacitive effective thickness, CET($|V| = 2.1$ V), for both n- and p-channel capacitors. $CET(V) = (\varepsilon_0 \kappa_{SiO2} A)/C(V)$; ε_0 is the permittivity of free space, κ_{SiO2} is the dielectric constant of SiO_2, and C(V) is the capacitance at bias voltage, V. There is a maximum difference (determined from comparing $\Delta d_{ox} = d_{ox}^{simulated}$ - EOT(Tqm_v6) for the various simulators) of 0.251 nm (0.220 nm) for p-channel (n-channel) devices simulated with d_{ox} = 2.0 nm. This discrepancy does not scale with thickness (the maximum difference is 0.238 nm (0.227 nm) when d_{ox} = 1.0 nm) and therefore is more problematic for thinner gate dielectrics.

One metric determining the exact outcome of a particular implementation of QM effects is the difference between CET simulated with and without QM effects

($\Delta CET = CET^{QM} - CET^{classical}$). Figure 2 shows ΔCET for three different simulators. This figure shows the result of modeling QM effects for these simulators, and quantitatively illustrates the (Å-scale) differences that arise between these implementations of QM.

Simulator	n-channel		p-channel	
	CET (nm)	EOT (nm)	CET (nm)	EOT (nm)
NCSU	2.465	1.836	2.461	1.828
NEMO (1.901 nm)	2.537	1.902	2.555	1.916
UTQuant	2.606	1.965	2.576	1.935
Berkeley	2.494	1.862	2.398	1.770
SCHRED	2.438	1.811	2.430	1.800
In-House	2.666	2.020	2.659	2.012

Table 1: Thickness parameters extracted by using Tqm_v6. d_{ox} = 2.0 nm (1.901 nm in NEMO), $N_d = 1 \times 10^{18}$ cm^{-3}, and $N_{poly} = 1 \times 10^{20}$ cm^{-3}.

There are many factors associated with the various modeling approaches and details of the physics that contribute to the observed differences. There are a number of ways to implement electron and hole quantization that can be divided into two primary categories: (1) simulations based on self-consistent solutions to the Schrödinger and Poisson equations, and (2) modification of the classical inversion and accumulation charge.

Some simulators in category (1) solve the Schrödinger equation throughout the entire structure while others limit the solution to the substrate and force the wave function to disappear at the interface. Wave-function penetration into the gate dielectric will cause higher predicted capacitances because the carriers are effectively closer to the interface. Recently, Mudanai, et al.[10] have reported this increased inversion-layer capacitance (of NMOSFETs) is insignificant except when $N_d \approx> 1 \times 10^{20}$ cm^{-3} and $d_{ox} <\approx 1.0$ nm.

Category (2) simulations can also be implemented in different ways. Some category (2) simulators modify the surface potential term in the classical calculations to include the extra band bending necessary to reach a given inversion or accumulation charge while others modify the bandgap near the interface by changing the intrinsic carrier concentration. The choice of carrier statistics when changing inversion and accumulation charge, i.e., Maxwell-Boltzmann (MB) or Fermi-Dirac (FD), leads to different results. This is most easily illustrated (Figure 3) for the classical, metal-gate, CV curves that are the starting baseline for category (2) simulators.

Currently, implementations of QM effects in 2D simulators are not as advanced as those found in many of the 1D simulators. In addition, QM effects are typically implemented as a locally 1D effect, and the role of true 2D quantization is yet to be determined. Benchmarking 2D simulators requires the development of a 2D structure to validate the 1D QM effects. Then it must be determined that these simulators effectively simulate 2D devices, properly accounting for effects such as fringe-fields and source/drain overlap. To achieve the first step, a 2D structure must be made large enough to emulate a 1D device. After a gate length calibration process, we found (for d_{ox} = 2.0 nm) that a 4 μm gate length MISFET is sufficiently long that the scaled capacitance per unit area has reached its 1D asymptotic limits

(demonstrated in Figure 4). Although the classical 2D and 1D CV curves show good agreement in the accumulation region and inversion region capacitance for both metal and poly-Si gate devices, the 2D simulators studied thus far do not have sufficiently accurate QM corrections to be compared with the 1D results.

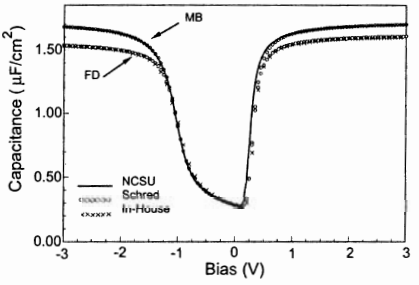

Figure 3: Classical CV curves with Fermi-Dirac (FD) statistics (Schred, in-house) and Maxwell-Boltzmann (MB) statistics (Schred, NCSU). n-channel, d_{ox} = 2.0 nm, Nd = 1 x 10^{18} cm^{-3}.

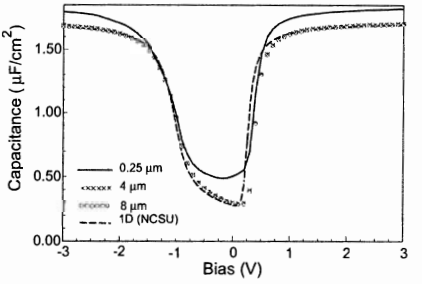

Figure 4: Scaled classical CV curves from 2D FETs as a function of gate length compared with 1D results. n-channel, d_{ox} = 2.0 nm, Nd = 1 x 10^{18} cm^{-3}.

4 Conclusions

We have performed an extensive comparison of QM CV simulators. As previously shown for n-channel devices, large differences (up to 20% for ultra-thin gate dielectrics) in the accumulation capacitance of p-channel capacitors are observed. We have illustrated some of the factors leading to this discrepancy. The observed differences are due to a complex interplay of many of these factors. Further improvements in QM corrections are needed in 2D simulators to emulate 1D MOS capacitors, and further work is required to develop an effective benchmark for 2D QM effects.

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