

Finite Element Simulation of 2D Quantum Effects in Ultra Short Channel MOSFETs with High-K Dielectric Gates

A. Poncet, B. Vergnet and M. Mouis

Laboratoire de Physique de la Matière, UMR-CNRS n° 5511, INSA-Lyon
20, Avenue Albert Einstein, F-69621 Villeurbanne, France
phone : (+33)4 72 43 87 30. e-mail poncet@lpm.insa-lyon.fr

Abstract - Ultra short channel MOS transistors with high permittivity gate dielectrics suffer from carrier quantum confinement in the channel and from electric field fringing in the dielectric layer. This paper deals with the 2D numerical simulation of the coupling between these two physical mechanisms. We shall demonstrate how they impact the threshold parameters in MOS transistors for metallurgical channel lengths ranging from 5 to 50 nanometers. A special attention has been paid to the control on numerical errors.

1 - Introduction

With the ultimate thinning of gate silicon dioxide layers, tunneling currents are becoming so large that going further in scaling-down requires new dielectric materials. HfO_2 for instance, increases the dielectric constant by one decade, and solutions are under investigation to get one decade more. These solutions will operate with channel lengths in the deca-nanometer range, leading to specific 2D effects, due to electric field fringing at gate edges which causes dramatic degradation of threshold voltages (V_t) and sub-threshold slopes (S) [3].

At the same time, quantum confinement in the channel may no longer be neglected. Carrier quantification has been extensively analyzed by means of numerical solutions of coupled Poisson and Schrödinger equations in 1D, in order to predict the impact of technological parameters on voltage-capacitance responses of *large* devices [1]. This has seldom been done for ultra-short gate MOSFETs [2], although device scaling rules would require a careful analysis of the couplings between quantum mechanical effects (QME) and short channel effects (SCE).

2- Numerical techniques

2-1 Finite elements

In this work, finite elements have been used to solve both Poisson and Schrödinger equations in 2D. This method is indeed especially well suited to analyze complex topographies. In addition, the Galerkin formulation of the equations makes the expression of most boundary conditions very straightforward. Vanishing probability current define boundary conditions along symmetry axes and ohmic contacts (unless carrier transport is not considered) which do not affect the hermitian nature of the Hamiltonian matrix. Transmission conditions, which are used to simulate wave function penetration into the gate dielectric, behave similarly .

Piecewise bilinear shape functions on quadrilateral elements were used in this work in order to highlight in a simple way the impact of mesh sizes near the silicon/dielectric interface. Meshes were graded on both sides perpendicularly to the interface, and constant in the lateral direction. Finite elements are worth being used with general purpose mesh generators, but we did not want to obscure the discussion by questions arising from local refinements or angle criteria.

2-2 Eigensystem

With finite elements, one has to face a 2-matrices eigenvalue problem, in which both matrices are equally sparse, unless the right-hand side matrix has been diagonalized by using a “mass-lumping” technique. Unfortunately, going further on, i.e. mapping this matrix to identity would break the symmetry of the Hamiltonian matrix. However, these are minor problems in comparison with non-sparse matrices arising from alternative methods based on Fourier series[5].

Simulating MOS devices in 2D brings another difficulty. As eigenvalues that are relevant to carrier quantification in the channel are fully mixed with those relative to source/drain areas [4], in contrast with the 1D case, it is necessary to sum up carrier densities over a large number of energy levels. This consumes both CPU time and storage space and it is mandatory to restrict the integration domain to its minimum.

2-3 Decoupling scheme

For solving Poisson and Schrödinger equations in a consistent way, fast decoupling schemes are required. Methods proposed in the literature are either slow (under-relaxation [5]) or difficult to implement (regula falsi [6]). Here, we implemented a new and very simple iterative scheme, which proved to be extremely fast : Once carrier densities have been deduced from eigen-energies and wave-functions, a “Fermi-like” potential is introduced and kept constant during Newton-Raphson iterations on Poisson’s equation. This potential is calculated using a Boltzmann statistics, although it has no physical meaning in the given situation : this should only be seen as a simple mathematical trick to benefit from the fast convergence of Newton methods. This does not prevent the final solution to obey Fermi-Dirac statistics, with the density of states relevant to the given degree of confinement. As depicted in figure 1 for a 1D NMOS capacitor, convergence is extremely fast at any regime. Convergence remains good in 2D, so that simulations with up to 1500 mesh nodes was found affordable, even on a desktop computer .

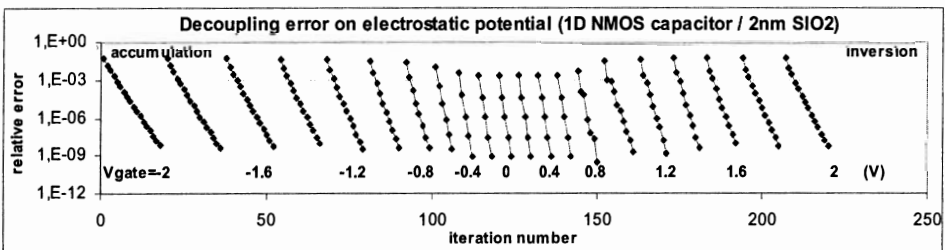


Figure 1 – Convergence of the decoupling scheme. 1D NMOS capacitor, with holes and electrons computation, from accumulation to inversion. Each symbol depicts one iteration.

2-4 Meshing constraints

The impact of the basic meshing parameters has been analyzed, with both classical and quantum models. Results can be summarized as follows :

- The impact of transverse mesh size in Si at the Si/dielectric interface is far higher when quantum effects are ignored (fig. 2). This is especially dramatic on capacitance values (fig. 2-b), and this can be related to the smoothing of carrier concentrations induced by their confinement in the vicinity of the interface.
- In short channel transistors, classical solutions are weakly sensitive to the lateral mesh size along the channel, but surprisingly, the quantum solutions are even less sensitive, especially with high-K dielectrics (fig. 3).

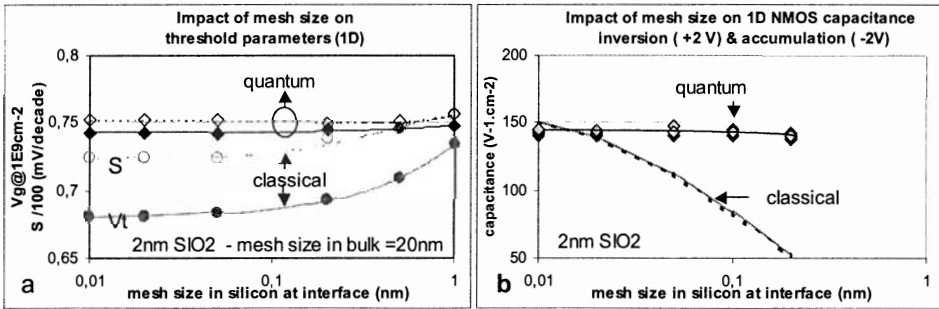


Figure 2 – Impact of *mesh size in silicon*, perpendicular to the channel at Si/SiO₂ interface 1D structure - 10¹⁸cm⁻³ channel doping - 2nm SiO₂ (a) on S and V_t (estimated at 10⁹cm⁻² in the channel) (b) on capacitance in accumulation (-2V) and inversion (+2V)

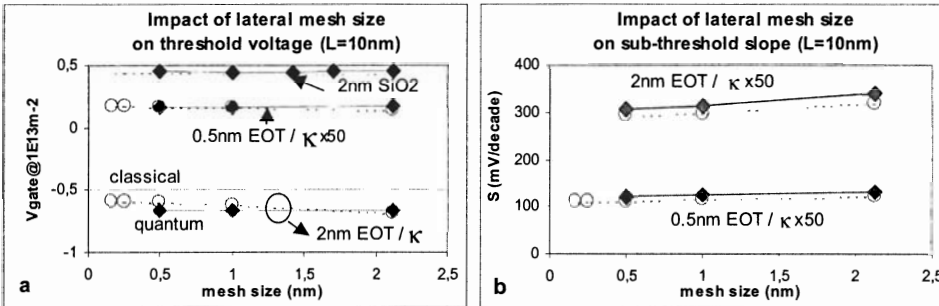


Figure 3 – Impact of the *lateral mesh size* - L_m=10nm, EOT=2nm.

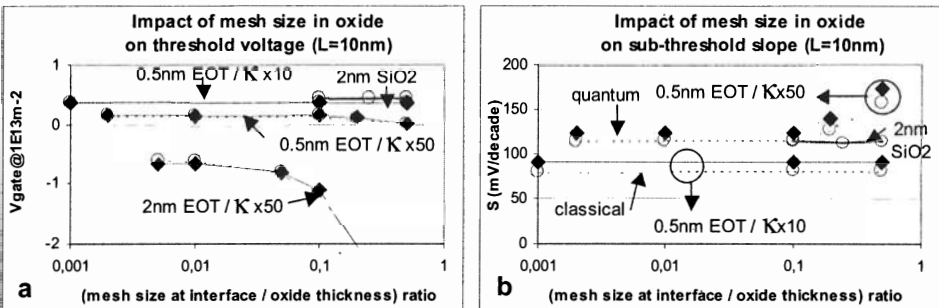


Figure 4 – Impact of the *transverse mesh size in the oxide* at Si/ SiO₂ interface, L_m= 10nm.

- The impact of the size of the simulated source/drain areas is weak as well (not shown here). It means that neglecting high frequency wave functions in the source or drain regions (because of a coarse lateral mesh) has a limited impact on carrier profiles in the channel and that the domain in which Schrödinger equation is to be solved can be shrunk without too much damage (keeping only 10nm apart from the ohmic contact edges has been proved to be sufficient).

- Using a too large transverse mesh size in the dielectric leads to over-estimate the degradation of V_t and S induced by a large thickness-to-length ratio (fig. 4).

3- Influence of channel length with high-K gates

The couplings between SCE and QME were analysed on NMOS transistors with metallurgical channel lengths (L_m) ranging from 5 to 50 nm and equivalent oxide thicknesses (EOT) from 0.5 to 2 nm. Dielectric constants were 1, 10 or 50 times larger

than SiO₂ one. Doping levels were 10^{18} , $2 \cdot 10^{19}$ and 10^{21} cm^{-2} in the channel, in the extensions and in the ohmic areas respectively. Simulations were performed with a fixed set of mesh size values : 0.5 nm lateral mesh size and graded transverse mesh with sizes ranging, in silicon, from 0.1nm at the interface to 50nm at bulk contact and, in the dielectric layer, from 1/100 to 1/4 of the layer thickness.

Our results agreed with simulations reported elsewhere [3], to predict large degradations of threshold parameters with increased permittivities. The major new information brought by our 2D simulations is that QME enhance SCE as follows :

V_t is underestimated by non-quantum models in long channel transistors, whereas it is overestimated for $L_m < 10 \text{ nm}$ (fig. 5-a). On the other hand, quantum effects enhance the sub-threshold slope S (fig. 5-b).

With materials such as HfO₂ ($\kappa \approx 30$), high permittivity and 2D carrier confinement have similar quantitative impacts on SCE; therefore, simulating the former while ignoring the later would be meaningless. Moreover, in contrast with the 1D case where QME reduce the carrier density at any regime, from accumulation to inversion (dotted line in fig. 6), the charge in ultra-short channels is only reduced in a narrow range of gate biases, from V_t to the weak-to-strong inversion transition.

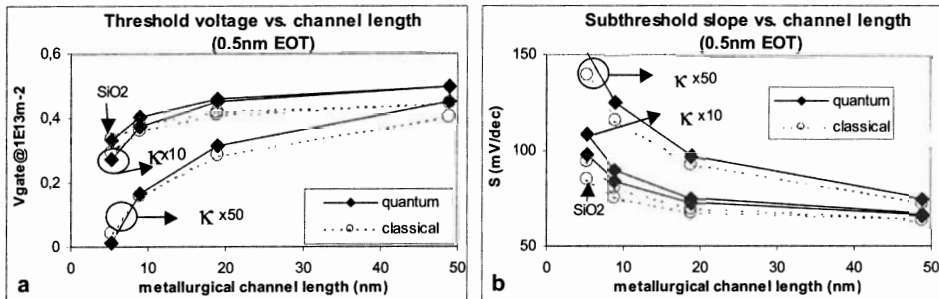
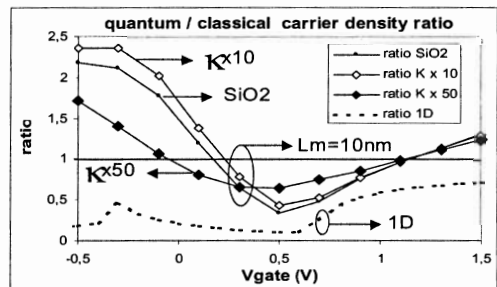


Figure 5 – NMOS threshold parameters versus L_m . Permittivity ratio vs. SiO₂ = 1, 10 and 50. EOT=0.5nm. (a) $V_t(L_m)$, (b) $S(L_m)$

Figure 6 - Quantum / classical ratio on carrier density versus gate voltage in NMOS transistors with $L_m=10 \text{ nm}$ and EOT=0.5nm. Permittivities are 1, 10 and 50 times SiO₂ one. The dotted line depicts the 1D case.



4- Conclusion

The combination of devices scaling down and of increasing speed and storage capabilities of desk-top computers makes numerical simulations of 2D quantum effects affordable for MOS device designers. It has been shown that ignoring these effects in the case of high-K dielectrics may lead to mis-interpretations of the sensitivity of the device characteristics with respect to process and design parameters.

References

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