# A Methodology for Deep Sub-Quartermicron CMOS Technology Characterization

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**Abstract**

We present a novel methodology for characterization of sub-quartermicron CMOS technologies. It involves process calibration, device calibration employing two-dimensional device simulation and automated Technology Computer Aided Design (TCAD) optimization, and, finally, transient mixed-mode device/circuit simulation. The proposed methodology was tested on 0.25 $\mu$m technology and applied to 0.13 $\mu$m technology in order to estimate ring oscillator speed. The simulation results show an excellent agreement with available experimental data.

## 1 Introduction

The manufacturing process with shrinking technology is becoming so complicated that using simulation in a predictive manner has been recognized as an integral part of any advanced technology development. In order to satisfy predictive capabilities the simulation tools must capture the process as well as device physics. Before going to production one can optimize the process steps and estimate device performance characteristics such as threshold voltage, saturation current, leakage current and circuit speed.

Several tools for simulation of semiconductor technology (e.g. [1, 2]) as well as semiconductor devices (e.g. [3]–[6]) are well established for device engineering applications. The two-dimensional device simulator MINIMOS-NT is equipped with an extensive mixed-mode circuit capability including modeling of distributed devices [7]. It works in an automated device optimization framework [8]. This allowed creation of a novel methodology for very deep sub-micron technology characterization.

## 2 Methodology

The technology characterization system implemented at LSI Logic has been successfully used for 0.25 $\mu$m and 0.18 $\mu$m technologies. It included technology process and device calibration using TSUPREM4 [1] and MEDICI [3], respectively, sensitivity analysis and Monte Carlo statistical analysis, and, finally, gate delay estimation using a compact physical model in HSPICE [9]. For 0.13 $\mu$m technology the HSPICE physical model failed to fit the I-V characteristics extracted by MEDICI and it was impossible to estimate the gate delay characteristic of that technology using the old methodology.

In our new approach the process calibration part is kept the same while device simulation is performed by MINIMOS-NT in the SIESTA optimization TCAD framework. The same distributed devices are then employed in a transient mixed-mode device-circuit simulation [7]. The gate length $L_g$, gate width $W_g$, optical gate oxide thickness $T_{ox}$, and applied voltage $V_{dd}$ for the investigated technologies are summarized in Table 1.

| Technology | $L_g$ | $W_g$ | $T_{ox}$ | $V_{dd}$ |
|---|---|---|---|---|
| 0.25 $\mu$m | 0.2-1.0 $\mu$m | 20 $\mu$m | 4.7 nm | 2.5 V |
| 0.13 $\mu$m | 0.115-0.7 $\mu$m | 10 $\mu$m | 2.3 nm | 1.5 V |

**Table 1:** Key parameters for the technologies considered in this work

## 2.1 Device Calibration

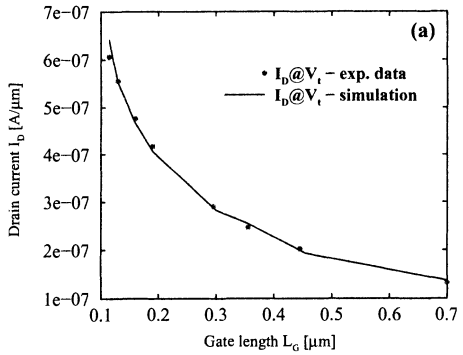
We use the SIESTA TCAD framework to perform an automated device calibration without user interaction during the optimization process. The setup allows simultaneous calibration of the saturation current $I_{D,sat}$ and the threshold voltage $V_t$ to the measured values for several devices of different gate lengths with a minimum global error [10]. For the 0.25 $\mu$m technology calibration, 11 NMOS and 11 PMOS devices and for 0.13 $\mu$m technology 8 devices of each type, respectively, were used. Only a few technology dependent physical model parameters which can vary with the process were used for calibration. Such parameters are the workfunction difference $E_w$ which is calibrated to account for the unknown density of surface states, or the surface mobility parameters $\mu_\nu^{\text{ref}}$, $S_\nu^{\text{ref}}$, and $\gamma_\nu$. The high-field mobility models are treated carefully, because their parameter values, e.g. the carrier saturation velocities $v_\nu^{sat}$ at 300 K generally must not be used as fitting parameters.

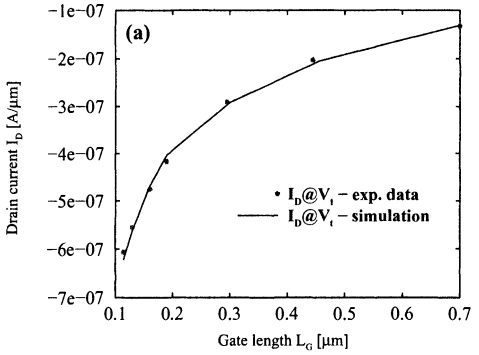
NMOS and PMOS device calibrations are performed separately because the model parameters are different. The proposed methodology of device calibration was tested on 0.25 $\mu$m technology. The new approach comprising of process calibration (TSUPREM4 - MEDICI) and device calibration (SIESTA - MINIMOS-NT) was applied to 0.13 $\mu$m technology. Device calibration was completed in about 8 CPU-hours. Good agreement with measured data was achieved both for the NMOS (Fig. 1) and for the PMOS (Fig. 2) devices. The final physical parameters from the optimization procedure are summarized in Table 2.

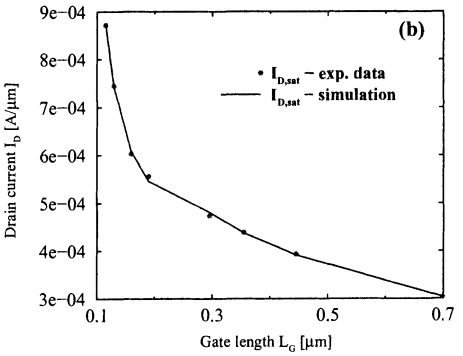
| | 0.25 $\mu$m | | 0.13 $\mu$m | |
|---|---|---|---|---|
| Parameter | NMOS | PMOS | NMOS | PMOS |
| $E_w$ [eV] | -0.372 | 0.551 | -0.433 | 0.407 |
| $\mu_\nu^{\text{ref}}$ [cm$^2$/Vs] | 582 | 78 | 573 | 82 |
| $S_\nu^{\text{ref}}$ [V/cm] | 5.4e5 | 6.6e5 | 6.3e5 | 6.2e5 |
| $\gamma_\nu$ | 7.1 | 8.0 | 6.0 | 8.7 |
| $\beta_\nu$ | 1.18 | 1.06 | 1.1 | 1.1 |
| $v_\nu^{sat}$ [cm/s] | 9.8e6 | 9.8e6 | 1.2e7 | 1.18e7 |

**Table 2:** Mobility model parameters for the 0.25 $\mu$m and 0.13 $\mu$m technologies

The agreement achieved is within 2% for $V_t$ and $I_{D,sat}$ versus gate length. All six model parameters remain close to their default values, while the saturation velocity resulting from the 0.13 $\mu$m technology calibration is $\sim$ 20% higher than the default value of $v_\nu^{sat} = 10^7$ cm/s. Therefore, we performed a comparative hydrodynamic (HD) simulation. A significant velocity overshoot governs the larger part of the channel area in the nominal 0.13 $\mu$m NMOS device compared to the overshoot observed in the 0.7 $\mu$m device. In drift-diffusion (DD) simulation this overshoot effect can be globally accounted for by increasing the $v_\nu^{sat}$ [11]. Such a change will only slightly influence the long channel devices, but will have a large effect on the short channel ones. Thus,



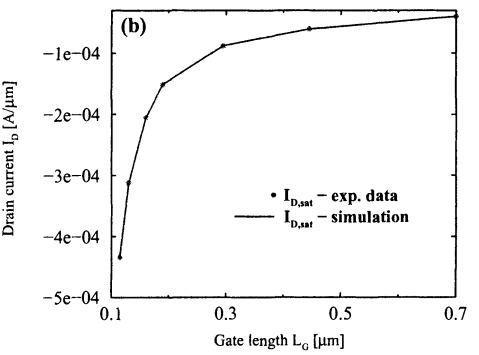




**Fig. 1:** Calibration of the threshold voltage $V_t$ (a) and the saturation current $I_{D,sat}$ (b) for NMOS devices created with 0.13 $\mu$m technology

**Fig. 2:** Calibration of the threshold voltage $V_t$ (a) and the saturation current $I_{D,sat}$ (b) for PMOS devices created with 0.13 $\mu$m technology

the high value of $v_\nu^{sat}$ in our calibration is justified considering that a DD simulation was performed.

## 2.2 Circuit Simulation

The calibrated model parameters were used for the circuit simulation. The ring oscillator simulation was carried out in transient mixed-mode using basic DD equations. The extracted gate delay for the 0.25 $\mu$m technology is 29.5 ps/stage which is in very good agreement with the experimental 32 ps/stage and with the 28.6 ps/stage extracted by the HSPICE physical model. To explore how many stages are sufficient to guarantee accurate results at minimum computational costs the ring oscillator circuits with three, five, and seven inverter stages were simulated. A simulation with five stages turned out to be sufficient to achieve the same results for the circuit speed as in simulations with more stages. The node voltages of the five stage ring oscillator circuit from the 0.13 $\mu$m technology are depicted in Fig. 3. The simulated inverter delay time is 15.2 ps/stage. In Fig. 4 the gate delay times extracted from several ring oscillators, each with 119 inverter stages (solid line represents the mean value) are compared with simulations (filled circles) performed for two calibrated wafers. The predicted gate delays are within the scattering range of the measured data.

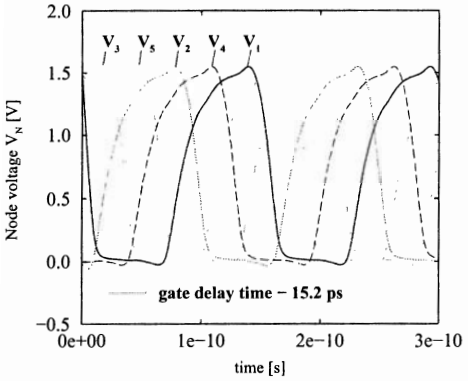



**Fig. 3:** The simulated node voltages of a five stage ring oscillator created with 0.13 $\mu$m technology

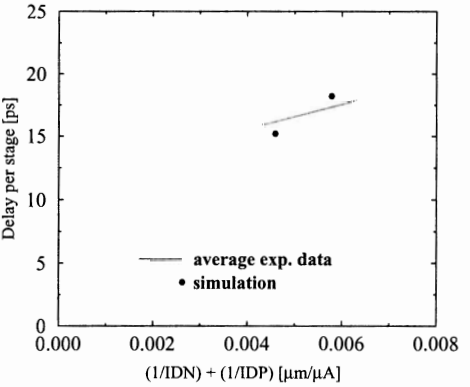



**Fig. 4:** The average experimental gate delay compared to simulation results obtained for two calibrated wafers

## 3 Conclusion

A new methodology was established for deep sub-quatermicron technology characterization. The new approach includes process calibration performed by TSUPREM4 - MEDICI, device calibration carried out by MINIMOS-NT in the SIESTA optimization framework and, finally, mixed-mode circuit simulation with distributed devices made by MINIMOS-NT. The methodology was tested and the tools were calibrated with a 0.25 $\mu$m technology. The approach was applied to a 0.13 $\mu$m technology characterization. Predicted ring oscillator speed is in excellent agreement with experimental data. The new methodology can be extremely beneficial in the early stages of process development for estimation of device performance.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