A Practical Approach to Modeling Strained Silicon NMOS Devices

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Abstract

Parameters for a generalized mobility model are extracted from hardware measurements of strained silicon NMOS devices. Only the phone limited mobility parameter was shown to vary with amount of strain in the silicon. Using results of the mobility model fitting, simulations of strained and unstrained silicon devices were performed. These simulations indicated that strained silicon devices should have improved short channel control as well as yield a minimum of 50% improvement in on current.

1. Introduction

It has been known for a long time that biaxial strain in silicon leads to higher mobility for in-plane transport of electrons [1,2]. Both the low and high field mobility are increased due to a splitting of the conduction band, resulting in a higher population of electrons in the lower energy valleys where they exhibit a lower effective mass. The most common and perhaps best developed method of creating a thin strained silicon layer is by growing a silicon layer on unstrained $Si_{1-x}Ge_x$ as demonstrated in [3]. In this work, we show a practical method for simulating strained silicon NMOS devices using standard drift-diffusion equations and a commonly used silicon mobility model that has been calibrated to low field (linear) Id-Vg hardware data. Using this calibration, we then simulate hypothetical sub 100 nm gate length strained silicon and conventional devices to compare expected DC performance, showing better short channel effect, Idlin and Ion for the strained silicon devices.

2. Low Field Mobility Calibration

Strained silicon and conventional long channel devices were fabricated and the linear I-V characteristics were measured. For the strained silicon devices, Ge content was fixed at either 15% or 20%. An approximate device structure was defined based on the process used to manufacture the devices, and Fielday [4] simulations were then performed. For both the control device and strained silicon devices, the Mujtaba mobility model [5] was used. The Ge content in the SiGe layer and strain in the silicon were taken into account by using appropriate band offsets in the defined device.

A Levenberg-Marquardt optimization program was used to adjust mobility model parameters to fit the Id-Vg hardware data. Since strained silicon should not necessarily exhibit the same mobility-field relationship as conventional silicon, we added two more adjustable parameters in the Mujtaba model. Within the phonon

limited mobility portion of the model, there are two terms dependent upon transverse field. One of these terms has the functional form: $C/(E_t^{\gamma 1})$, with $\gamma 1=1/3$. The surface roughness limited mobility portion of the model has a term which shows the functional form: $\delta/(E_t^{\gamma 2})$, with $\gamma 2 = 2$. The two parameters that we used as adjustable ones were $\gamma 1$ and $\gamma 2$. In addition to $\gamma 1$ and $\gamma 2$, we also fit the δ and C parameters. During the optimization procedure, we found that $\gamma 1$ and $\gamma 2$ changed by less than 5% from their original values and that the surface roughness mobility term, δ also changed by less than 5%. This tells us that the low field mobility improvement is due to changes in phonon scattering and that surface roughness scattering is not affected much by strain. For higher transverse electric fields than for those shown here it is expected that the surface roughness scattering term will have a large impact [7], and for strained silicon devices the surface roughness limited mobility is expected to be larger than that for conventional silicon devices.

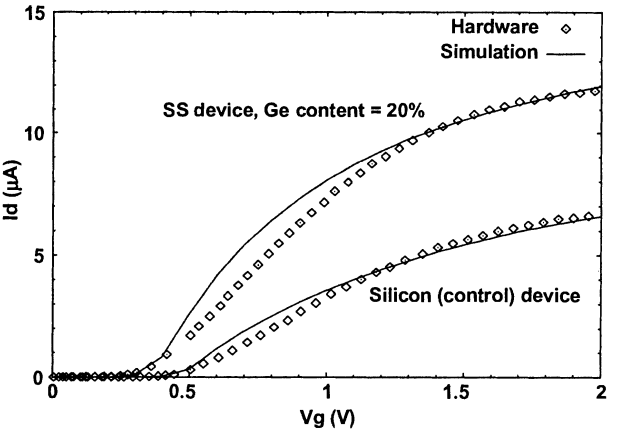

Fig. 1. Comparison of measured and simulated linear Id-Vg characteristics of 10X10 strained and unstrained silicon devices.

Table 1. Normalized values of C extracted from optimization.

Device	Ge content	C (normalized)
Control	0%	1.0
SS	15%	2.7
SS	20%	4.0

The only parameter that had a significant impact on the fit was the phonon limited mobility parameter, C. Figure 1 shows the fit compared to hardware data for the silicon control device and the strained silicon device with a Ge content of 20%. A similar fit was performed to device characteristics with 15% Ge content. The values of C (normalized to the silicon control device) are shown in Table 1. To a reasonable approximation, the phonon limited mobility is proportional to the Ge content of the unstrained SiGe layer. Since the biaxial strain in the thin silicon layer is linearly proportional to the Ge content, the phonon limited mobility can be seen to be proportional to strain. The fit of the simulations to hardware is certainly not as good as it can be. Taking into account a more detailed understanding of the device structure including S/D resistance and poly depletion effects and using additional mobility parameters would improve the match, but our intent here is to show feasibility using a conventional silicon mobility model and its application to device design.

3. DC Device Performance Improvements

We define a generic sub 100 nm process such that the off current is 10 nA/μm for the shortest channel length device (80nm). Although Ge content and strain will affect the dopant distribution in actual devices [6], we assume that the doping profiles in both sets of devices follow the same shape. Power supply was set to 1.5 V. We compare a control (silicon) device to a strained silicon device with Ge content of 20%. For high field mobility considerations, [1] shows that velocity saturation in silicon is 1.07×10^7 cm/sec and in $Si_{0.8}Ge_{0.2}$, Vsat = 1.3×10^7 cm/sec. Figure 2 shows the Vt roll off characteristics of these prototype devices. There is a lot of roll up in the characteristics due to the relatively heavy halo that was defined. Figure 3 shows the ratio of Idlin for the various gate lengths. For long channel lengths, we see an improvement in Idlin of greater than the mobility improvement of 75% due to the strain. The additional improvement in Idlin is due to Vtlin of the strained silicon devices being less than that of the control devices. For shorter channel lengths, the difference in Vtlin is less and the halo doping in the strained silicon devices is starting to affect the channel mobility. Figure 4 shows the Ion/Ioff characteristics. A significant improvement in on current can be obtained using strained silicon devices. Higher off currents for long channel devices are due to higher junction leakage in the strained silicon devices.

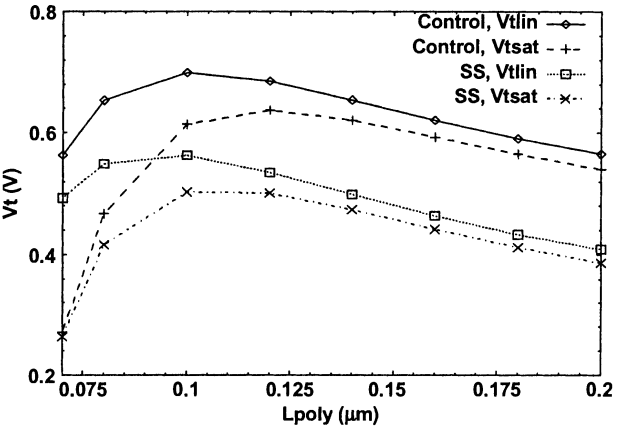

Fig. 2. Vt roll off characteristics of the control and strained silicon devices. Vtsat for the 70 nm gate length devices are similar due to the constraint of off current being 10 nA/μm.

Devices designed around nominal gate length should be compared to look at important differences between strained silicon and conventional device design. Because we constrain the off current at minimum channel length to be 10 nA/μm, Vtsat for minimum device length are the same. Due to band

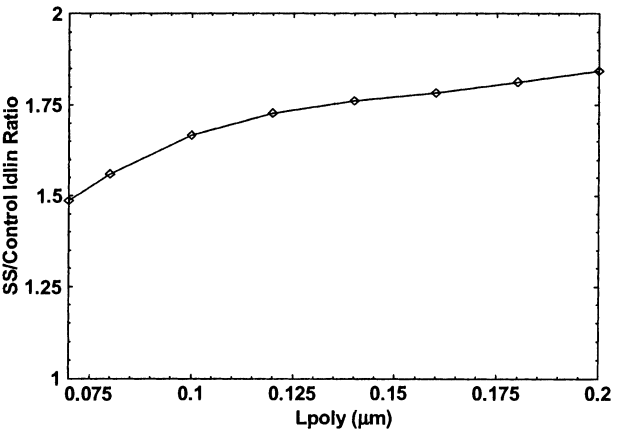

Fig. 3. Ratio of linear current for strained silicon and control devices as a function of gate length.

offsets in the strained silicon layer, Vtsat is shifted to a lower value than a conventional device with the same doping profile. To compensate for this, the background doping in strained silicon devices must increase, yielding better control over short channel effects. For a nominal gate length of $0.1\,\mu$ m, Vtsat of the strained silicon device is approximately 100 mV lower than the conventional device. Because of the lower Vt and higher saturation velocity we see an Ion improvement of ~50%. We can also see that short channel effect is improved significantly for strained silicon devices.

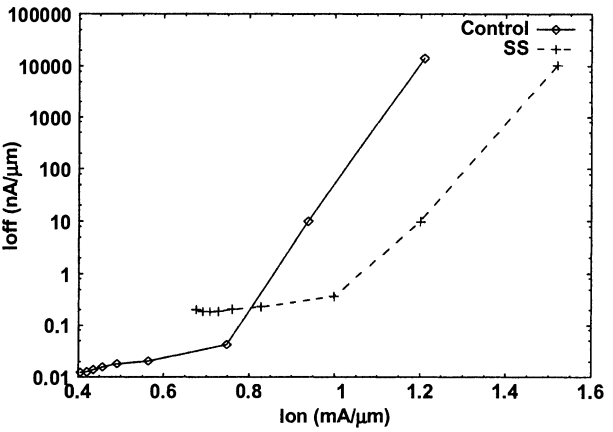

Fig. 4. Ion/Ioff characteristics of the control and strained silicon devices. Significantly higher on currents can be obtained using strained silicon. Off currents for long channel length strained silicon devices are larger than the control devices due to higher junction leakage.

4. Conclusions

A simple and effective method to simulate strained silicon devices was shown. A simple calibration showed that phonon limited mobility in strained silicon will be significantly better than conventional silicon devices. It was also seen that the field dependence of the mobility is comparable in strained silicon devices to that of conventional devices. Even though typical low field mobility improvements of 75% for 20% Ge content SS devices have been seen, greater than 75% improvement in Idlin can be obtained due to a lower Vtlin of the strained silicon devices. Better short channel effects and on currents can be obtained due to effects of band offsets and doping profiles in the strained silicon devices.

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