TCAD Driven Process Design of 0.15μm Fully-Depleted SOI Transistor for Low Power Applications

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Abstract

We presented a TCAD-driven total design methodology of FD-SOI MOSFETs, starting from 0.35μm/2.5V shrinking to 0.15μm/1.5V. Jumping from 0.35μm to 0.15μm, two-phase experiments are performed effectively supported by exhaustive applications of TCAD local models. SOI specific consideration of SOI film thickness variations (σTsoi) and floating-body effects are the key points for the TCAD driven strategy.

1 Introduction

Silicon-on-insulator(SOI) is a promising technology for low power applications. Especially, fully-depleted (FD) SOI MOSFET has advantages in short channel effects and subthreshold characteristics. In deep sub-micron region, however, trade-off relationships of FD-SOI MOSFETs are more complicated than those of bulk transistors. Therefore TCAD-driven process design would be more efficient in FDSOI cases. In this paper, TCAD-driven total design methodology of SOI MOSFETs, starting from 0.35μm/2.5V shrinking to 0.15μm/1.5V, is presented. SOI specific consideration of SOI film thickness variations (σTsoi) and floating-body effects are the key points for the TCAD driven strategy.

2 Fabrication Process

The commercially available SIMOX wafers with 100nm-thick buried oxide are used as the starting material. The starting Tsoi is about 60nm and the final Tsoi is thinned down to 40nm. Gate oxide (electrical thickness Tgox:4nm) is grown after a LOCOS isolation. After gate pattering and spacer formation, a cobalt-silicide process is applied to reduce the source-drain sheet resistance.

3 TCAD driven development of 0.15μm FD-SOI transistor

In 0.15μm FDSOI transistor development, we focus on the power consumption in view of supply voltage reduction (requirement: Vdd=1.5V) maintaining the Ion-Ioff(@Vd=2.5V) of the preceding generation 0.35μm FD-SOI. In order to keep process compatibility for quick development, the basic well process sequences of

0.35μm FD-SOI transistor are inherited. Our TCAD driven process design methodology of 0.15μm FD-SOI transistor consists of the following 3 steps (Fig.1).

3.1 Certifying overall process strategy with 0.35um SOI models (phase-0)

Fig.2 shows the calibration results of 0.35μm SOI. Using this calibration model, we estimate short channel effects and Ion-Vdd trends before developing 0.15μm SOI. Fig.3 shows the simulated Ion trends having the same Ioff for FD-SOI devices. On the basis of this outlook for device scaling and Vdd reduction, basic scaling directions (Tgox=4nm, Tsoi=40nm) are determined.

3.2 Building basic Vth window considering σVth effects (phase-1)

In first-step experiment, we construct the response surface functions(RSFs). The RSFs can be used for the following 3 purposes: (A) Making rough process windows (B) Estimating device performance variation (C) Obtaining experimental data for local model refinement [1] to optimize the process conditions. TCAD calibration model of the preceding generation is effective for estimating process control parameters range (Fig.4: as for (A)). Also the variation of device performance due to process variations (considering σTsoi, σTgox, σLgate and σVtdose) is predictable (Fig.5: as for (B)). In order to clarify the effect of σTsoi, we obtain σVth extracted from RSFs (Fig.6). As Fig.6 shows, the behavior of σVth-Tsoi varies significantly as Lgate is varied. The behavior specific to FD-SOI devices are caused by the combination of Tsoi variations and short channel effects. In this case (Tsoi=40nm), it is revealed that the influence of σTsoi is smaller than that of short channel effect. Process optimization based on (C) is discussed in 3.3 .

3.3 Optimization of extension/halo considering floating-body effects (phase-2)

In this optimization step, the refined TCAD calibration model is used for more precise device performance prediction even if process parameters are extrapolated. In 0.15μm SOI process, LDD structure, which is adopted in 0.35μm SOI for suppressing floating-body effects, cannot satisfy the Ion-Ioff requirements for 1.5V Vdd. Furthermore, it is difficult to keep a fully-depleted state at long Lgate, especially in low-Ioff requirement (<0.01nA/μm). In order to overcome this situation, extension/HALO process is adopted in 0.15μm SOI process. As refined-model predicted, S/D extension increases the Ion compared to LDD (Fig.7) because of suppressing parasitic source-drain resistance, and HALO implant can effectively suppress to be partially-depleted state at long channel (Fig.8) without thinning Tsoi and/or heavier channel doping. On the other hand, as Ion are increased, BVsd is decreased because the impact-ionization and floating-body effects are enhanced. Especially in FD-SOI devices, such phenomena are also influenced by the change of Vt-rolloffs which are due to the variations of Tsoi and Lgate. In order to maximize the Ion under the specifications of BVsd, we optimized the process considering the effect of σTsoi and σLgate by using TCAD (Fig.9).

4 Device Performance

Fig.10 shows that 0.15μm FD-SOI devices have the advantage of bulk devices having the same Tgox and Ioff. Fig.11 shows the fabricated IdVd characteristics of 0.35μm SOI and 0.15μm SOI transistor (having the same Ioff). As we expected, the supply voltage of 0.15μm SOI can be successfully decreased while maintaining the Ion-Ioff of 0.35μm SOI.

5 Summary

We presented a TCAD-driven total design methodology of FD-SOI MOSFETs, starting from 0.35μm/2.5V shrinking to 0.15μm/1.5V. 0.15μm FD-SOI MOSFETs are successfully optimized in short time by the TCAD-driven process design. Jumping from 0.35μm to 0.15μm, two-phase experiments are performed effectively supported by exhaustive applications of TCAD local models. TCAD advantages specific to FDSOI MOSFETs design are as follows:

a) The effects of σTsoi on σVth are clarified in the 1st Vth window step.

b) Considering σTsoi, BVsd limited by floating-body effects are optimized in the 2nd extension/HALO optimization step.

References

[1] Mar, J. (1996): The Application of TCAD in Industry. In: Proceedings of International Conference on Simulation of Semiconductor Process and Devices, SISPAD' 96, Tokyo. Japan Society of Applied Physics, Tokyo, pp.139-145

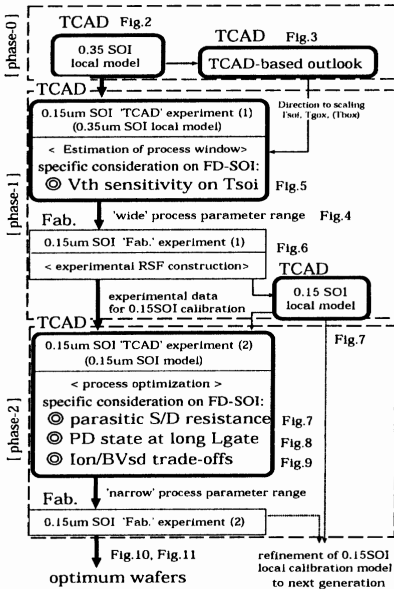

Fig.1. Procedure to concurrent TCAD driven 0.15um FD-SOI transistor development.

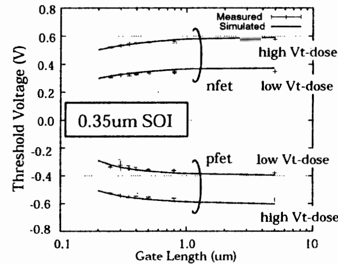

Fig.2. 0.35um FD-SOI calibration results.

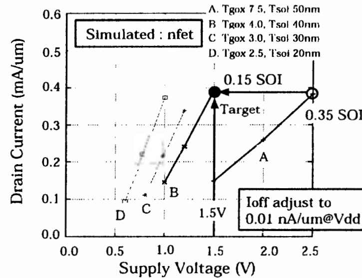

Fig.3. Simulated Ion trends having the same Ioff FD-SOI devices.

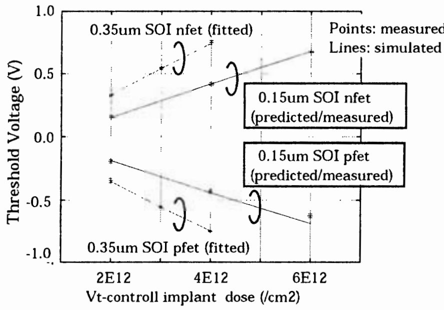

Fig.4. Vt-Implant dose dependence of Vth.

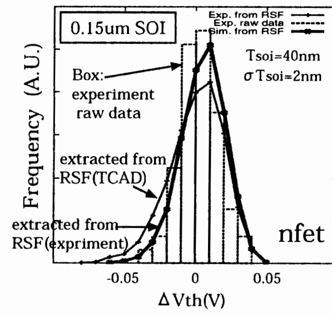

Fig.5. 0.15um SOI Vth distributions.

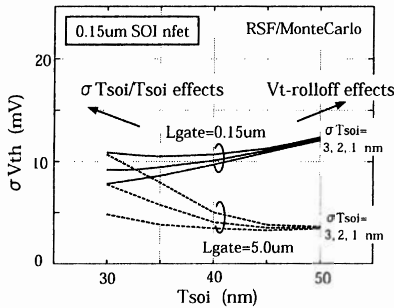

Fig.6. σVth v.s. Tsoi for σTsoi=1,2,3nm

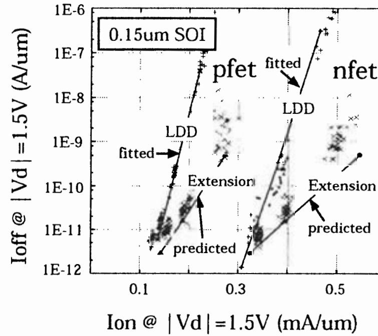

Fig.7. 0.15um SOI: Ion-Ioff characteristics.

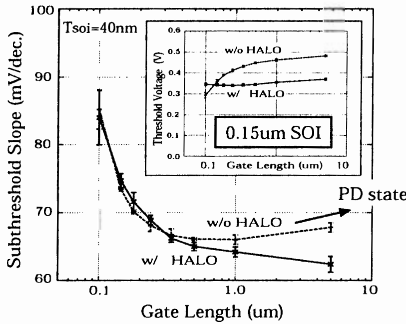

Fig.8. Subthreshold slope for nfet.

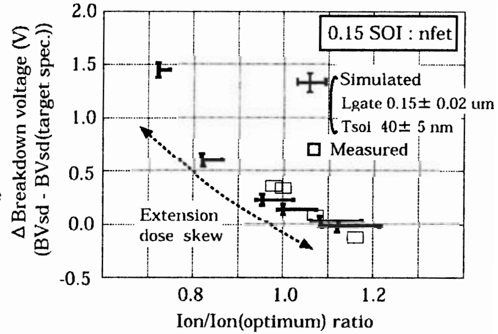

Fig.9. BVsd v.s. Ion considering σTsoi and σLg.

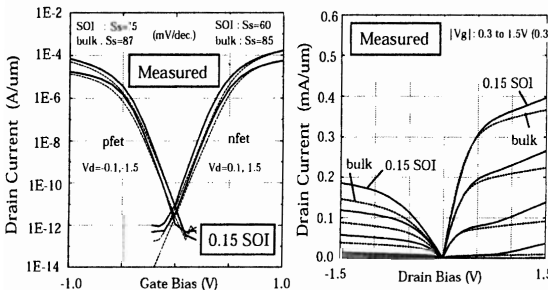

Fig.10. IdVg and IdVd characteristics of fabricated 0.15um FD-SOI and bulk (Tox_inv=4nm).

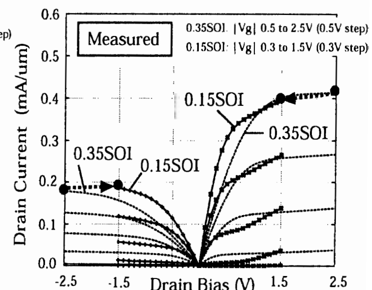

Fig.11. IdVd characteristics of 0.35um SOI and 0.15um SOI.