Device Simulation and Measurement of Hybrid SBTT

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Abstract

A hybrid Schottky barrier tunneling transistor is assessed by device simulations and measurements. n^+ regions are formed in Schottky contact regions of source and drain. The unified simulation technique is used to simulate ohmic and Schottky contact natures. The devices are fabricated by utilizing the conventional extension process. It is shown that potential modulation by n^+ regions reduces drain leakage current and enhance the tunneling probability at the source contract.

1 Introduction

The Schottky Barrier Tunneling Transistor (SBTT) has been studied as one of candidates for sub-0.1μm MOSFET structure (Tucker et al. 1994) because of its immunity to the short channel effect (SCE). However, there are problems, namely the high source contact resistance and the high leak current of majority carriers at the drain electrode. In this work, a Hybrid SBTT (HSBTT) designed to suppress the problems was assessed by device simulations and measurements.

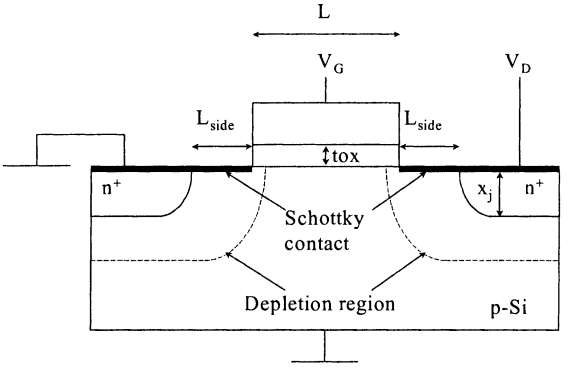

Fig. 1. Schematic of HSBTT.

2 Device simulation of HSBTT

Fig. 1 shows a schematic of the HSBTT. The potential distribution around the edge of the Schottky electrode is modulated by n^+ region. In order to carry out device

simulations for the structure, the unified simulation technique for ohmic and Schottky contacts (Matsuzawa et al. 2000) was necessary. Fig. 2 shows the forward bias characteristics of a Schottky barrier diode (SBD) simulated by using the contact model. It was confirmed that the results for SBD get nearer to those of ideal ohmic contact as the impurity concentration increases. Fig. 3 shows the gate bias dependence of the drain current for three kinds of MOSFETs. Although the SCE immunity of HSBTT is inferior to that of SBTT, it is superior to that of the conventional MOSFETs. $ErSi_2$ was used in the simulations as the Schottky contact to reduce the source contact resistance for electrons. It was found that the resistance could be reduced also by adding n^+ region to the source contact region, which is shown experimentally in the following section. Fig. 4 shows the gate bias dependence of the substrate current. The substrate current of HSBTT is one-order lower than that of SBTT. This is because the depletion region spreading from the drain n^+ region relaxes the electric field around the drain electrode and suppresses the tunneling of holes.

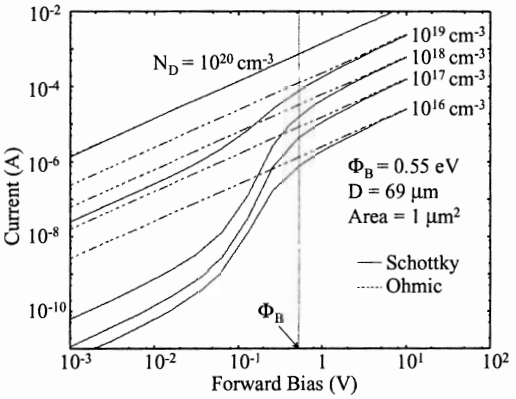

Fig. 2. Forward bias characteristics of SBD.

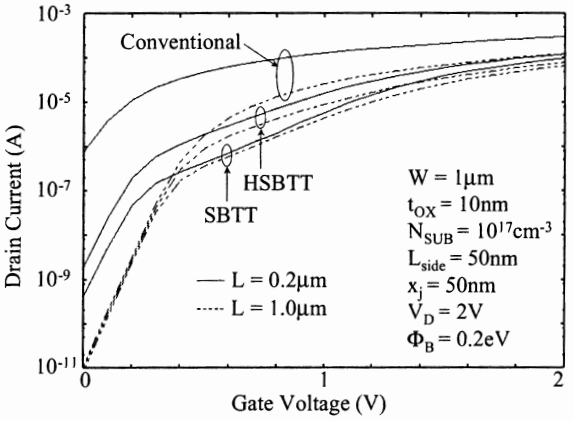

Fig. 3. Gate bias dependence of drain current for three kinds of MOSFETs.

3 Measurement of HSBTT

Fig. 5 shows the fabrication process of HSBTT using a typical material, $TiSi_2$, in our clean room. The distance between the edge of n^+ regions and the edge of source/drain electrodes L_{side} was controlled by the deposition thickness of the polysilicon, t_{poly}. It was confirmed that the fabricated Schottky contact exhibited a reasonable rectifying characteristic, as shown in Fig. 6. Fig. 7 shows measurements of the gate bias dependence of the source current. The SCE of HSBTT is sufficiently suppressed comparing with that of the extension structure. It was found that the source current of HSBTT could be controlled by t_{poly}. This is because the depletion region spreading from the n^+ region modulates the shape of the tunneling barrier at the source electrode and the potential profile depends on L_{side} as shown in Fig. 8.

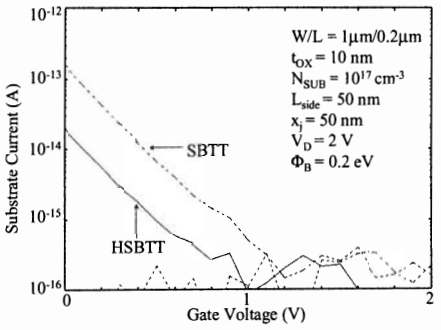

Fig. 4. Gate bias dependence of substrate current for SBTT and HSBTT.

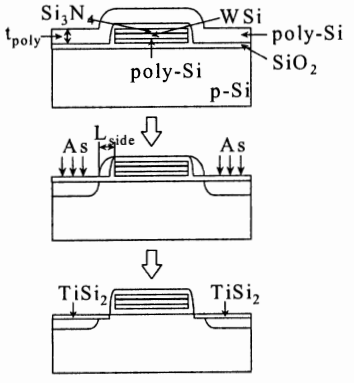

Fig. 5. Fabrication process of HSBTT.

4 Conclusion

The electrical characteristics of HSBTT were assessed by device simulations and measurements. The immunity of HSBTT to the short channel effect was superior to that of the conventional MOSFET. The source contact resistance was controlled by the position of the high impurity region in the Schottky electrode region. The leak current at the drain electrode of HSBTT was one-order lower than that of SBTT.

References

[1] Tucker, J.R., Chinlee Wang, Carney, P.S. Silicon field-effect transistor based on quantum tunneling. Appl. Phys. Lett. 1994; 65: 618-620

[2] Matsuzawa, K. Uchida, K. Nishiyama, A. A unified simulation of Schottky and ohmic contacts. IEEE Trans. Electron Devices 2000; 47: 103-108

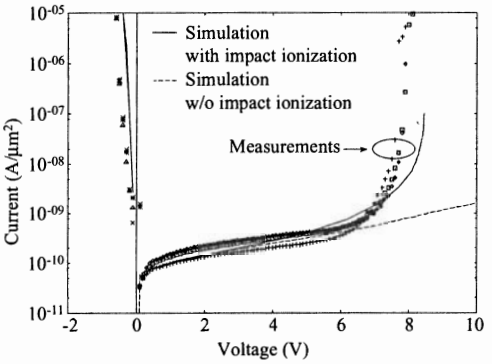

Fig. 6. Rectifying characteristic of fabricated Schottky contact.

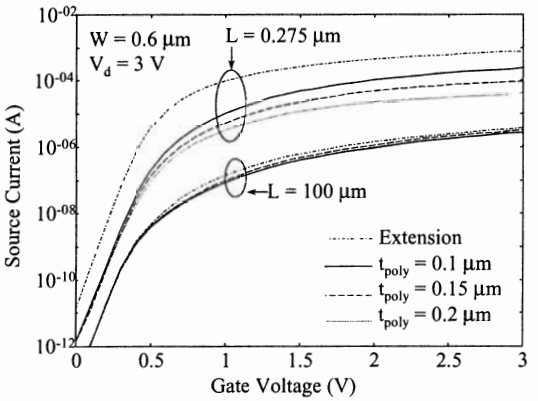

Fig. 7. Gate bias dependence of source current for fabricated HSBTT.

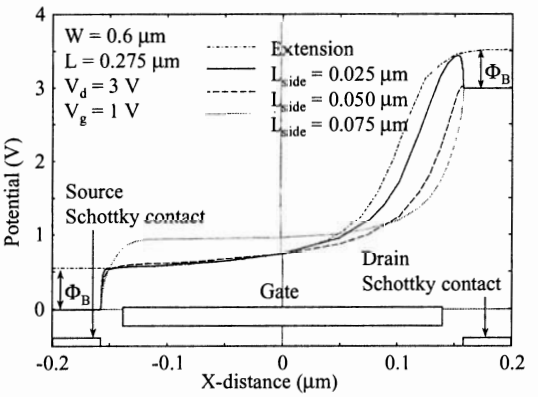

Fig. 8. Potential distribution at substrate surface.