Simulation of Flash Memory Programming Characteristics

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Abstract

A practical approach is presented to simulate programming characteristics of Flash memories. The current continuity equation for carriers injected in SiO_2 is embedded in the Poisson equation. The amount of hot electrons at the interface of substrate and SiO_2 is used as the fixed boundary condition for NOR-Flash, whereas spatial distribution of the FN tunnelling probability in SiO_2 is considered for NAND-Flash.

1 Introduction

In many cases of simulations for programming characteristics of NOR- and NAND-Flash memories, the capacitance value around the floating gate (FG) has been necessary (Lorenzini et al. 1999, Kim et al. 1998). However, it is sometimes troublesome to determine the value. In the present approach, the current continuity equation for carriers injected in SiO_2 is embedded in the Poisson equation around FG instead of specifying the capacitance value. The programming characteristics by hot electrons and FN tunneling are demonstrated.

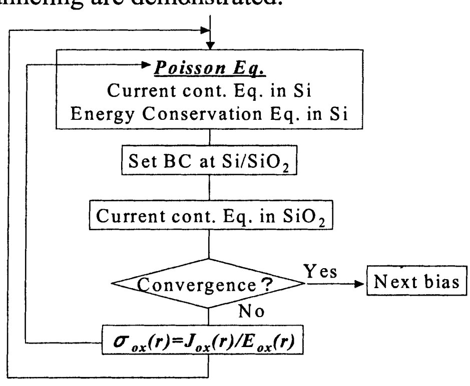

Fig. 1. A flowchart for simulation of programming characteristics of NOR-Flash.

2 Programming for NOR-Flash

Fig. 1 shows a flowchart for simulation of the hot electron programming of NOR-Flash in the present approach. First, the amount of hot electrons is estimated by solving the energy conservation equation in the silicon region. Then, distribution of current density around FG is obtained by solving the current continuity equation in the SiO_2 region. Distribution of electric conductivity around FG is calculated and the current continuity equation composed of current density J_{OX} in the SiO_2, J_{FG} in FG, and displacement current density J_{DISP} is set up around FG as shown in Fig. 2. The continuity equation can be solved in the framework of the Poisson solver, since all the current densities are expressed by gradient of the potential ψ. Fig. 3 shows a schematic of behavior of hot electrons injected in SiO_2. The amount of the hot electrons that surmount the energy barrier is used as the fixed boundary condition for the current continuity equation in SiO_2 and then the distribution of hot electrons injected into SiO_2 is obtained as shown in Fig. 4.

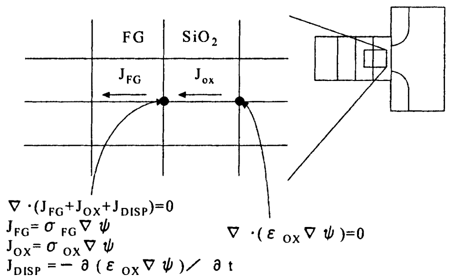

Fig. 2. Current continuity equation at the interface of FG and SiO_2.

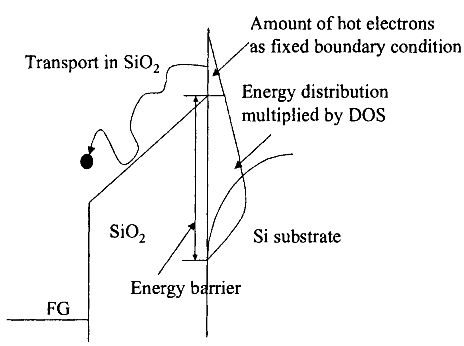

Fig. 3. Schematic of hot electron behavior in SiO_2.

Fig. 5 shows influences of the drain voltage V_D and the control gate voltage on the transient behavior of FG voltage V_{FG}. Ultimately, V_{FG} becomes lower as V_D is higher, since more hot electrons are generated. On the other hand, the ultimate value of V_{FG} tends to become the same value under the same V_D condition even if V_{CG} is different. This is because the combination of the gate current and V_{FG} tends to balance under the constant energy supply, namely the drain voltage.

3 Programming for NAND- Flash

Fig. 6 shows a schematic of FN tunneling. The tunneling probability was calculated based on the WKB approximation, considering the energy band gap in the floating gate and the substrate. Fig.7 shows the generation rate distribution of carriers in SiO_2 caused by the FN tunneling from the substrate under a programming condition. The gap of the distribution is due to the energy band gap of the substrate. It was found that the energy band gap affects the transient of V_{FG} as shown in Fig. 8.

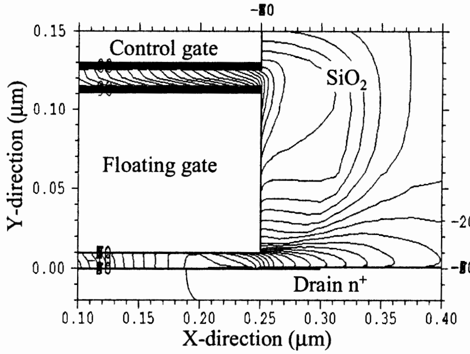

Fig. 4. Electron distribution injected into SiO_2.

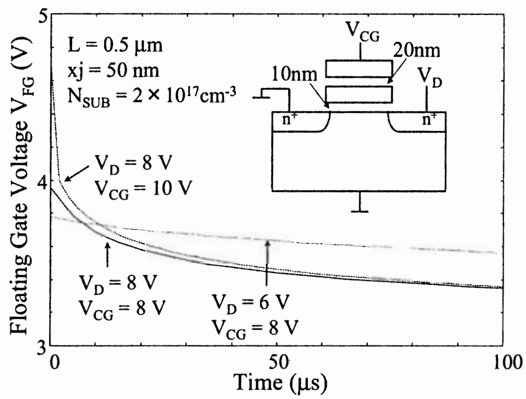

Fig. 5. Writing characteristics of NOR-EEPROM.

4 Conclusion

It is demonstrated that it is possible to simulate the programming characteristics of NOR- and NAND-Flash memories by embedding the current continuity equation for carriers injected into SiO_2 in the Poisson equation. The present approach allows us to simulate the characteristics self-consistently without specifying the capacitance value. Therefore, we expect that it can become a practical TCAD tool.

Acknowledgement

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References

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[2] Kim, D.M., Cho, M.K., Kwon, W.HStacked gate mid-channel injection Flash EEPROM cell- Part II: Analysis of gate current and modeling of programming characteristics. IEEE Trans. Electron Devices 1998; 45: 1703-1709

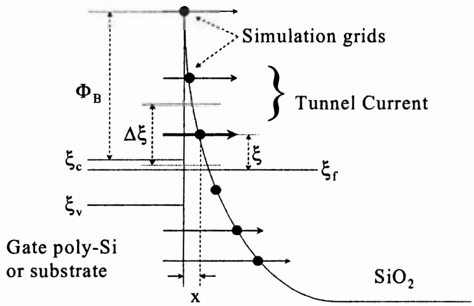

Fig. 6. Schematic of FN tunneling.

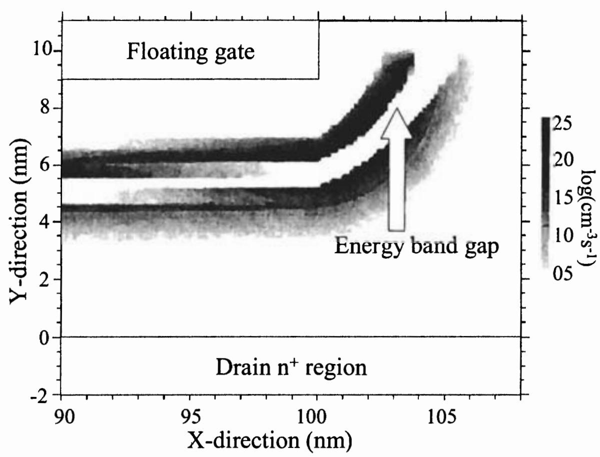

Fig. 7. Generation rate distribution by FN tunneling.

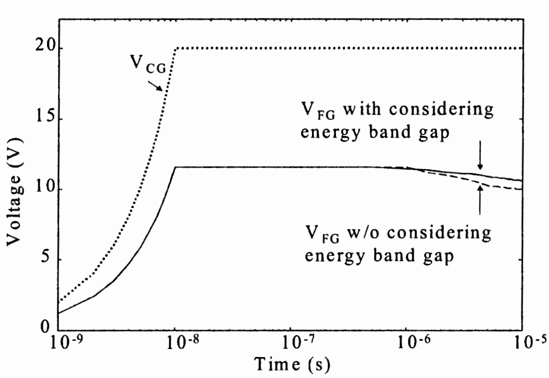

Fig. 8. Writing characteristics of NAND-Flash with similar parameters to those in Fig. 5.