A New Compact Spice-like Model of E²PROM Memory Cells Suitable for DC and Transient Simulations

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Abstract

This paper presents for the first time a new compact Spice-like model of a E²PROM Memory Cells suitable for both DC and transient circuit simulations. This model is based on a new Floating Gate voltage calculation procedure that improves strongly the accuracy of the modeling of the cell. Moreover, this model features many advantages compared to the previous ones: i) it is simple to implement and scale; ii) its computational time is not critical; iii) its parameter extraction procedure is the same of a MOS transistor; iv) it can be easily upgraded to take into account leakage current contributions (SILC).

1 The Model

Models of Floating Gate devices proposed in the literature are mostly based on the "classic" lumped element description of the FG cell shown in Fig.1(a). Memory operations are described starting from the exact knowledge of FG voltage, V_{FG}, which is calculated through fixed capacitive coupling coefficients, as reported in the paper of Pavan et al. (1997).

$$V_{FG} = \alpha_{CG} V_{CG} + \alpha_D V_D + \alpha_S V_S + \alpha_B V_B$$

However, these coefficients are not easy to measure, since the FG node cannot be directly accessed, and they depend on the applied terminal voltages, as stated by Duane et al. (1998). Therefore, considering them as constants introduces errors in the FG voltage calculation, thus compromising the correct model of the cell. For this reason, we have developed a new V_{FG} calculation procedure, which does not use fixed coefficients. As shown in Fig.1(b), the model we propose is composed by four elements: a MOS transistor whose Source, Body, Drain are S, B, D, of the cell, and Gate is the FG of the cell; a capacitor connected between FG and Control Gate; a voltage-controlled voltage source, V_{FG}, between FG and ground, which implements the V_{FG} calculation procedure and has been necessary to overcome the problem of simulating a capacitive net in DC conditions; a voltage-controlled current source, $I_{W/E}$, connected between FG and D, to reproduce write/erase transient currents. The new V_{FG} calculation procedure represents the core of our model and has been implemented in the C code routine controlling the voltage controlled voltage source. It is based on the solution of the charge balance equation at the FG node. That is, the sum of the charge on the MOS gate, Q_G, plus the charge on the bottom plate of C_{CG}, has to be equal to the charge forced in/out the floating gate during cell program/erase operations, Q_{FG}, which in DC condition is a constant and depends on the state of the cell (for example,

$Q_{FG}\approx 11.5fC$ and $Q_{FG}\approx -4fC$, for an erased and written cell, respectively). Q_G is a complex function of the S, B, D, FG voltages, whose analytical expression has been obtained from the charge equations of the MOS compact transistor model adopted (in our case: Philips MOS Model 9, www.semiconductors.philips.com/Philips_Models/).

$$Q_G(V_{FG}, V_S, V_D, V_B) + C_{CG}(V_{FG} - V_{CG}) = Q_{FG}$$

The voltage-controlled current source, $I_{W/E}$, has been implemented by a C code routine to reproduce write and erase currents. As known, write and erase of a E^2PROM cell occur by Fowler-Nordheim tunnel across the thin oxide between D and FG of the cell. The oxide field has been calculated by means of a self consistent model taking into account poly-depletion as well as charge quantization effects, which has been developed by Larcher et al. (2001). Results obtained by this model has been parameterized on the oxide thickness, the p-Si substrate and the n-well D doping. In this way, the model can successfully evaluate the correct oxide field for different device parameters and voltage combinations.

2 Results

The model proposed in this paper allows to reproduce accurately the whole electrical behavior of E^2PROM memory cells (W=0.3μm, L=0.75μm and C_{GC}=3fF) manufactured in the existing technology (0.25μm) by ST-Microelectronics. In Figs.2-3, examples of fitting capabilities of our model are shown in DC conditions compared to experimental data. The agreement between measurements and simulations is excellent without the need of any free parameter to adjust fitting quality. Only a small amount of charge has been assumed on the Floating Gate node, which is probably due to charging effects during the manufacturing process of the cell. Moreover, this model is able to simulate very accurately also the transient behavior of E^2PROM (see Figs.4(a)-(d)). Particularly, threshold voltage shifts occurring during both write and erase operations are excellently fitted without calibrating any additional parameters (see Figs.4(a)-(b)), and the use of this model allows to inspect and monitor physical quantities like the FG voltage and the erase current which cannot be directly measured (see Figs.4(c)-(d)).

3 Conclusions

In this paper a new Spice-like compact model of a E^2PROM cell has been proposed. It allows the reproduction of the whole electrical behavior (DC and transient conditions) of the memory cell with great accuracy, and it features new great advantages compared to previous models. 1) It is based on a new procedure which improves strongly the FG voltage estimate, as well as the whole modeling of the cell. 2) It is very simple to implement, since it uses standard circuit elements whose parameters can be determined by applying the MOS parameter extraction procedure to the dummy cell (FG and Control Gate are short-circuited). The only additional parameter is the capacitance between FG and CG, C_{CG}. 3) This model is easily scalable, since the compact MOS model already takes the scaling rules into account and they do not influence the V_{FG}

calculation procedure. 4) The write/erase current source can be changed or upgraded independently of the other parts of the model, thus enabling future development the description of W/E mechanisms as well as the inclusion of leakage current contributions (SILC). 5) The accuracy of the model depends on the compact MOS model adopted, thus taking advantage of the many efforts to improve and scale the MOS compact models.

References

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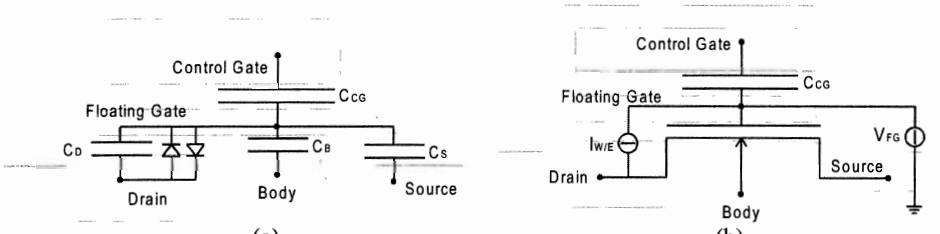

Fig.1. Previous lumped element equivalent model (a) and new compact Spice-like model (b) of a E^2PROM memory cell.

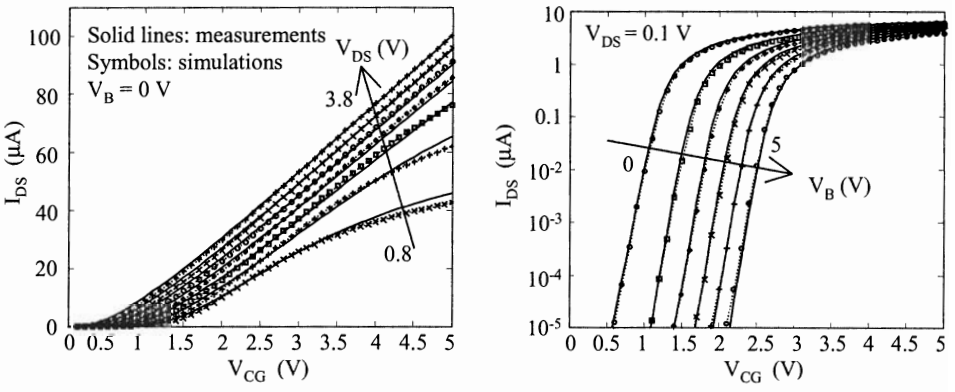

Fig.2. Measurements (solid lines) and simulations (symbols) on a E^2PROM cell (W=0.3μm, L=0.75μm and C_{GC}=3fF) in DC conditions: (a) trans-characteristics I_{DS}-V_{CG} parameterized on V_{DS}; (b) sub-threshold trans-characteristics I_{DS}-V_{CG} parameterized on V_B.

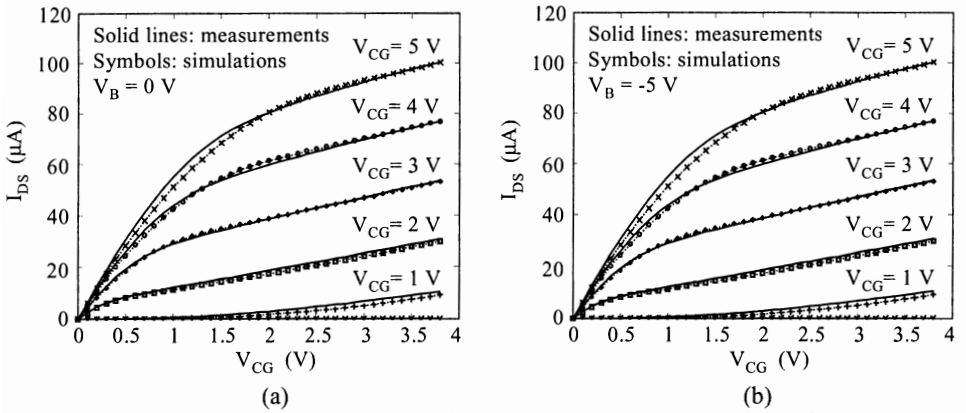

Fig.3. Measured (solid lines) and simulated (symbols) I_{DS}-V_{DS} characteristics for V_B=0V (a) and V_B=-5V (b) of a E^2PROM cell (W=0.3μm, L=0.75μm and C_{GC}=3fF) in DC conditions.

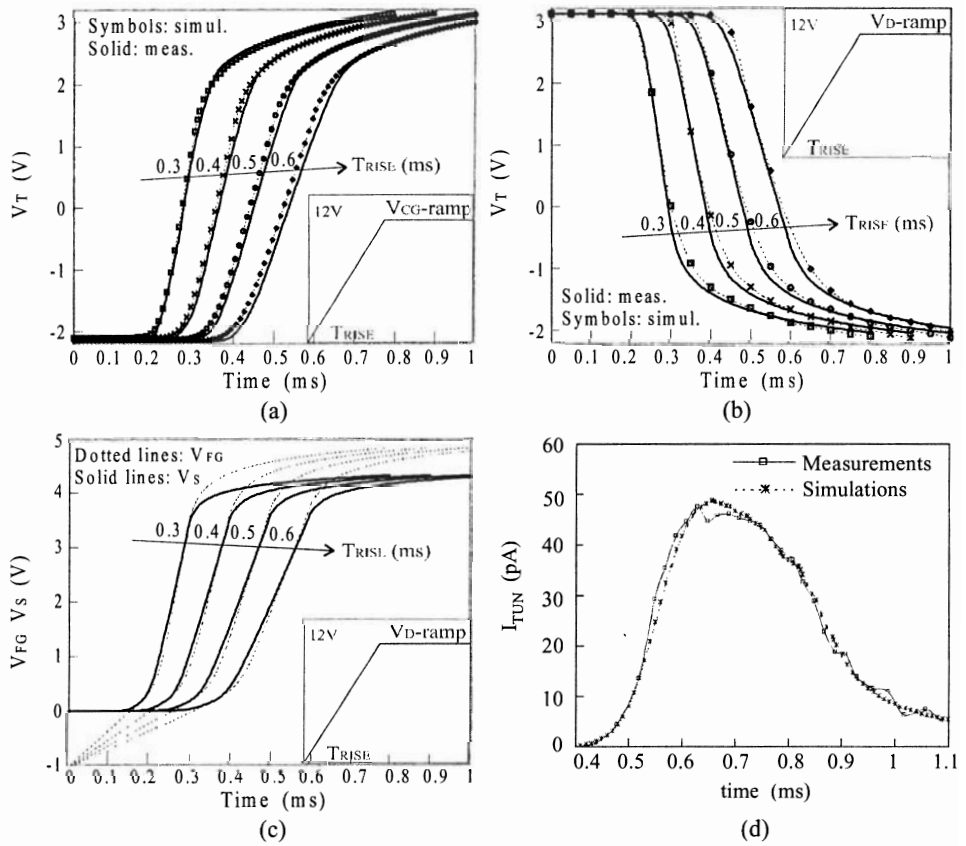

Fig.4. Measurements (lines) and simulations (symbols) of the threshold voltage shift in erase (a) (V_D=V_S=V_B=0V, V_{CG}-ramps) and write (b) transients (V_{CG}=V_B=0V, V_D-ramps, S floating); (c) simulations of V_S (solid lines) and V_{FG} (dotted lines) during a write transients and of the Fowler-Nordheim current, I_{TUN}, during the erase of the cell.