Analysis of Statistical Fluctuations due to Line Edge Roughness in sub-0.1μm MOSFETs

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Abstract

We present a full-3D statistical analysis of line edge roughness (LER) in sub-0.1 μm MOSFETs. The modelling approach for line edges and the parameters used in the analysis take into account the statistical nature of the roughness. The results indicate that intrinsic fluctuations in MOSFETs due to LER become comparable in size to random dopant effects and can seriously inhibit scaling below 50 nm.

1. Introduction

The intrinsic fluctuations in sub-0.1μm devices are normally associated with random dopant effects [1,2] and oxide thickness fluctuations [3]. However, as a random departure from the perfect geometry due to tolerances found in *every* lithography process, line edge roughness (LER) also introduces such intrinsic parameter fluctuations. Earlier works investigating the impact of LER in device simulations have been limited in terms of realism and sophistication. They all approximate LER in a 'square-wave' fashion in deterministic simulations [4,5] or employ faster 2D device simulations in a simplistic statistical approach [6]. In this work, we present a realistic 3D statistical approach to the simulation of LER in decanano MOSFETs. In the simulations LER is specified in terms of statistical parameters, *i.e.* rms amplitude (Δ) and correlation length (Λ). This allows both 3D and statistical aspects of LER to be naturally incorporated in a single simulation framework. We demonstrate the impact of LER in MOSFET scaling and show that it can further limit the integration of sub-0.1 μm MOSFETs, unless reduced significantly both in amplitude and correlation length.

2. LER Description and Model

Total LER amplitude is traditionally defined to be 3Δ, where the rms amplitude Δ of LER can be statistically obtained by inspection of lines generated by a given lithography process. Although not a new phenomenon, LER is rarely accounted for in device analysis, since the critical dimensions are at least an order of magnitude larger than the roughness in present day devices. However, as the aggressive scaling of Si-MOSFETs continues, LER of fixed amplitude may constitute an increasingly significant fraction of the gate length. Indeed, at the end of the Roadmap proposed by SIA [7], MOSFETs as small as 30 nm or less are anticipated. Data collected from different processes, summarised in Fig.1 attest to, at present, a minimum total LER limit of 5 to 6 nm (i.e. $\Delta \approx 2$ nm). This value, larger than the Roadmap requirement for devices below 100 nm, is alarming since metrology requirements are often more difficult to meet than actual line-width specifications for a given process.

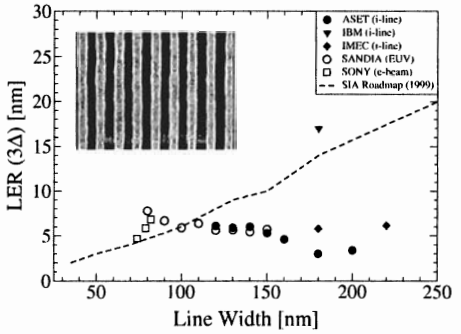

Fig.1. LER found in advanced lithography processes by various labs [6-12] and required by SIA roadmap (SIA) The inset shows LER found in sub-100 nm e-beam generated lines.

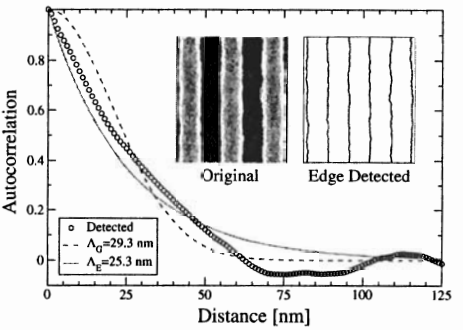

Fig.2. Autocorrelation of LER captured from 100 nm EUV lines. Correlation lengths obtained from Gaussian (Λ_G) and exponential (Λ_E) fits and detected edges are also given.

In contrast with rms values, significantly less is known regarding the correlation length of LER, which is reported to vary between 10 nm and 50 nm [7]. Our recent analysis on actual LER data obtained from EUV [8] and e-beam [9] lithography processes (see Fig. 2) indicate that typically Λ is approximately 30 nm. It is reasonable to assume that Λ may be reduced at higher resolution, which can utilise special resists and/or advanced exposure techniques for better LER performance. Gaussian and exponential models are found to perform equally well as least square fits to the captured autocorrelation data.

With reliable statistical data at hand, we reconstruct realistic source/drain junctions in 3D MOSFET simulations using a 1D Fourier synthesis approach. First a complex array with N elements is constructed, whose amplitude is determined by the power spectrum obtained from the adopted autocorrelation function. The phases of the elements are selected randomly, making each line unique. However, only (N/2 –2) elements of the array are independent. The rest are obtained by symmetry operations imposed so that, after inverse Fourier transform, the resulting height function *H(x)* is real. Random line examples generated using this method are given in Fig.3 for typical values of Δ and Λ. Lines with a Gaussian autocorrelation are smoother due to a lack of high frequency components in this model, as also can be seen in Fig.3.

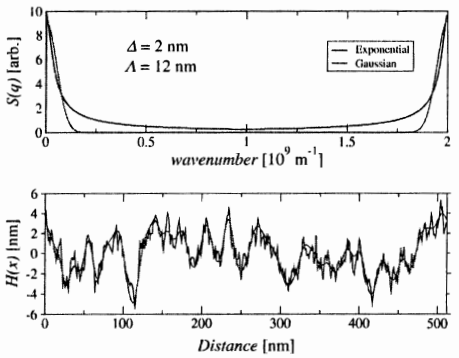

Fig.3. LER model used in the 3D device simulator. Both the power spectra (top) and actual random lines (bottom) are shown.

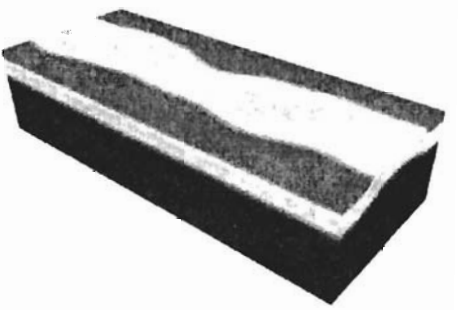

Fig.4. A typical 50x200 nm MOSFET used in 3D simulations. LER has parameters Λ=20 nm and Δ=3 nm.

3. Device Simulator

We employ the same 3D device simulator as in an earlier work investigating random dopant and oxide thickness fluctuation effects [2,3]. The LER modelling unit was incorporated within this to generate random junction patterns, without any numerical penalties owing to efficient FFT subroutines used in line generation. Throughout this work, ensembles of 200 MOSFETs with identical design parameters but unique junction patterns, such as the one in Fig.4, are simulated for statistical analysis. Unless indicated otherwise, Δ=2 nm and Λ=20 nm for all cases considered.

For the sake of simplicity and speed we use the drift-diffusion approximation, with constant mobility [2], and neither the quantum mechanical nor the atomistic doping options are enabled during simulations. A set of 200 devices takes 0.5–4 days to run on a single processor depending on the bias conditions, although in practice several processors are used in parallel. This is in marked comparison with 3 months reported for 70 MOSFETs by Oldiges *et al.* [6]. Using this efficient simulator, we focus on the variation of threshold voltage, V_T, leakage current, I_{off}, and drive current, I_{on}. Devices considered here comply with scaling requirements at each technology node and assume a Gaussian autocorrelation for LER used to construct the junctions.

4. Results and Discussion

Complementary to threshold fluctuations, LER causes fluctuations in drain on-state current, I_{on}, as can be seen in Fig.5. It is interesting to note that current distributions disclose a slight skew, which may be attributed to increased short channel effects in shorter elements of the ensemble. We verified that largest (smallest) I_{on} value in the distributions correspond to the device with the shortest (longest) effective gate length. For given device dimensions the standard deviation of threshold voltage fluctuations due to LER increase when Λ or Δ is increased. The latter dependence is given in Fig.6 for 30 and 50 nm MOSFETs. The inset in this figure plots the average threshold voltage lowering ($\langle V_T \rangle - V_{T0}$), where V_{T0} is calculated without LER. Thus, LER not only causes fluctuations but also lowers the threshold and its impact on threshold becomes larger as gate dimensions are reduced. Moreover, the fluctuations are comparable in magnitude to those resulting from random dopants in similar 30×30 nm devices studied by Asenov [2].

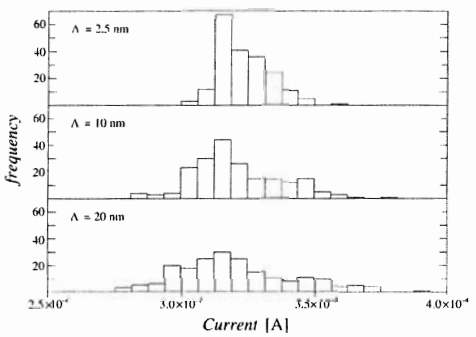

Fig.5. Histograms showing drain on-current distribution in 200 (30×30 nm) MOSFETs for three correlation lengths. The skew is due to short channel effects.

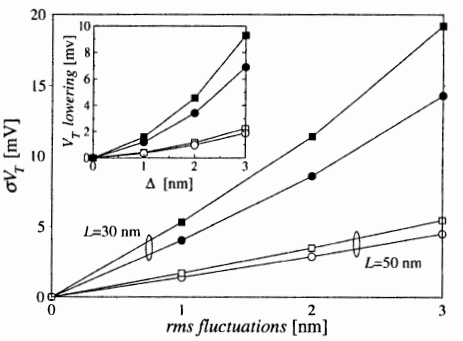

Fig.6. Standard deviation of threshold voltage for two decanano MOSFETs as a function of rms fluctuations at V_D=1.0V (squares) and V_D=0.1V (circles).

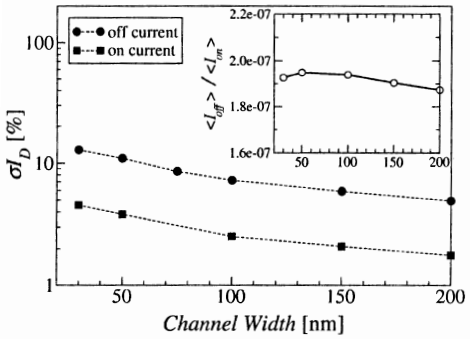

Fig.7. σI_D as a function of effective channel width in decanano MOSFETs. The inset shows ratio of average off- and on-currents. V_D=1.0 V, L_{eff}=50 nm, Δ=2 nm and Λ=20 nm.

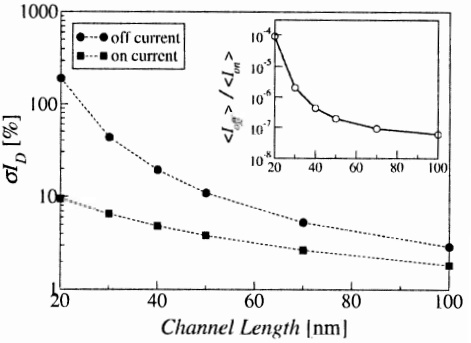

Fig.8. Dependence of drain current standard deviation on the effective gate length in decanano MOSFETs. The inset shows ratio of average off- and on-currents.

Fig.7 and Fig.8 display the dependence of the standard deviation of drain current on MOSFET gate width, W_{eff}, and length, L_{eff}, respectively for typical LER parameters. Both the on- and off-current dependencies are given for comparison. Clearly the W_{eff} dependence is an order of magnitude weaker than the L_{eff} dependence. Wider devices provide a progressively better average for the properties affected by the LER, thus reducing the uncertainty. The disproportionately large L_{eff} dependence is due to acute short channel effects in regions with drastic reduction in the local channel length introduced by LER. The simulated dependence becomes especially severe for devices with a gate length below 50 nm. Naturally in all cases off-current dependence is found to be more susceptible to the presence of LER.

The insets of Figs. 7 & 8 plot the ratio of average off-current to on-current. Since the average on-current remains relatively constant (see Fig.5), the ratio essentially provides a measure for the increased LER induced leakage. As in the case of standard deviation, the leakage current appears to be extremely sensitive to LER in MOSFETs with a gate length less than 50 nm. The width dependence of the same figure of merit is not significant, remaining below 5% overall. Therefore, both LER amplitude and correlation length must be reduced below the current projected minima to prevent excess leakage and fluctuations in MOSFETs with gate dimensions below 50 nm.

References

[1] Stolk, P A *et al.*, *IEEE Trans. Elec. Dev.*, **45**, 1960, (1998)
[2] Asenov, A, *IEEE Trans. Elec. Dev.*, **45**, 2505, (1998)
[3] Asenov, A and Kaya, S, *Proc. SISPAD*, Seattle, USA, 135, (2000)
[4] Linton, T, Giles, M and Packan, P, *Silicon Nanoelectr. Workshop*, 82, (1998)
[5] Linton, T, Yu, S and Shaheed, R, *VLSI Design*, in press.
[6] Oldiges, P *et al.*, *Proc. SISPAD*, Seattle, USA, 131, (2000)
[7] SIA, SIA Roadmap–Lithography, 147, (1999)
[8] Cardinale, G *et al.*, *J. Vac. Sci. Tech. B*, **17**, 2970, (1999)
[9] Thoms, S, Macintyre, D and McCarthy, M, *Microelec. Eng.*, **41/42**, 207, (1998)
[10] Mori, S *et al.*, *J. Vac. Sci. Technol. B*, **16**, 3739. (1998)
[11] Winkelmeier S *et al.*, *Proc. SPIE*, in press.
[12] Yoshizawa, M and Moriya, S, *Electr. Lett.*, **36**, 90, (2000)