3D Thermal Analysis for SOI and its impact on Circuit Performance

R. V. Joshi, [1]S. S. Kang, and C. T. Chuang
[1]IBM, Rochester, MN - 55901
IBM, T. J. Watson Res. Center, Yorktown Heights, NY - 10598
(rvjoshi@us.ibm.com, 914-945-1118)

Abstract

3D-thermal analysis for multifinger devices is developed for partially depleted SOI and Cu interconnects. Using this technique the temperature rise for multifinger devices is at least a factor of 3 higher than predicted by 1-D thermal resistance models.
Also increase in temperature degrades the performance incrementally.

1. Introduction

As silicon process technology, driven by improved performance requirements, migrates to SOI, low resistivity metals and low-k dielectrics, the thermal properties of these materials play a significant role in determining the temperature build-up, power and performance of the chip. In this work we have evaluated the temperature rise in high duty cycle critical circuits using 3-D thermal analysis for the first time.

2. Model/Simulation

The steady state temperature distribution of a multi-finger NFET with a realistic physical geometry in a clock buffer was studied using a commercial 3-D finite-difference thermal code. The geometry of a four-finger FET on a chip including the body, source and drain MCBAR as a local interconnect, gate polysilicon, five layers of metal, vias and dielectric was modeled in cartesian coordinates.

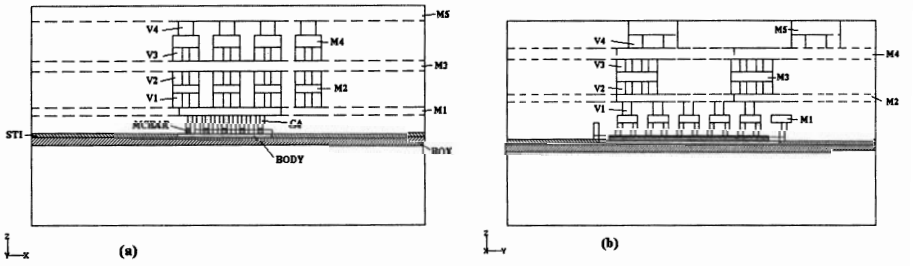

Figure 1 (a) and (b) show the geometry of the 20x20x11 μm region modeled.

The temperature field was determined by numerically solving the three dimensional Poisson equation for temperature. Heat dissipation was specified in the volume occupied by the channel region of the FET and in the five levels of metal lines based on circuit simulations for a clock buffer. Adiabatic (or symmetry) boundary conditions were specified on all the x and y boundary planes. A fixed chip temperature T=1 °C was specified on the z boundary 4 μm below the body of the FET while a fixed thermal conductance ($k=T|_z = C(T-T_o)$) to a surface (e.g. a chip carrier) at T_o =1 °C was specified on the z boundary at the last metal to mimic thermal conduction through a solder bump with a thermal resistance of 700 °C/W. A nine-finger FET was modeled by starting the FET body at the x=0 boundary and adding a half wide channel at that boundary.

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[1] Presently with Aavid Thernalloy LLC, Concord, NH 03301.

The calculations for the bulk technology were done by eliminating the BOX layer in the model. The physical design dimensions and materials considered are summarised in Table 1.

Layer	Thickness (μm)	Width (μm)	Material	Thermal Conductivity (W/m-°C)	Volumetric heating (mW/μm^3)
BOX	0.4		SiO_2	1.4	
STI	0.2		SiO_2	1.4	
Body	0.2		Si	120	
Channel	0.1	0.15	Si	120	0.06**
PC	0.2	0.26	Silicide	40	
MCBAR	0.3	0.25	Tungsten	170	
CA	0.6	0.25	Tungsten	170	
M1	0.4	1.1	Cu / Al	390 / 210	0.0136
V1	0.7	0.44	Cu / Al	390 / 210	
M2	0.4	1.35	Cu / Al	390 / 210	0.0218
V2	0.7	0.5	Cu / Al	390 / 210	
M3	0.5	2.24	Cu / Al	390 / 210	0.0268
V3	0.7	0.5	Cu / Al	390 / 210	
M4	0.6	1.35	Cu / Al	390 / 210	0.0444
V4	0.7	0.75	Cu / Al	390 / 210	
M5	0.8	2.6	Cu / Al	390 / 210	0.0154

**heat dissipation per μm of channel width.

Table 1. Physical design used in the thermal model.

Thermal simulations were carried out for a range of one to nine active fingers, SOI and bulk device, copper metalization, and silicon dioxide back end dielectric. Circuit performance simulations were likewise carried out using SPICE models with p(pfet) L*eff*=0.15 μm and n(nfet) L*eff*=0.12 μm.

3. Results and Discussions

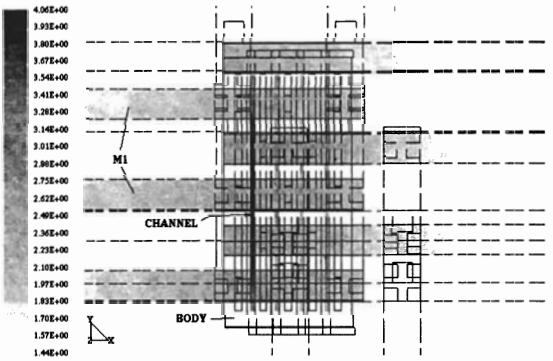

Figure 2. Junction and level 1 metal (M1) peak temperature rise in the SOI device with one active finger.

Only the leftmost channel is active and shows the highest temperature rise. The normalized junction-to-chip temperature rise or thermal resistance is 50 °C-μm/mW (3 °C rise for 0.06 mW/μm heat dissipation). Values reported in the literature range from 50-90 °C-μm/mW for single-finger devices with similar dimensions [1-2].

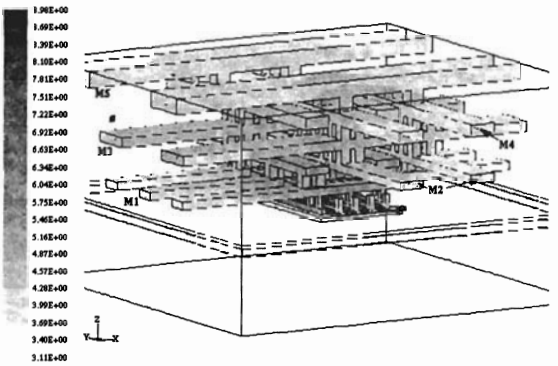

Figure 3. Illustrates the temperature distribution in all the metal interconnect (MCBAR to M5) with four fingers active.

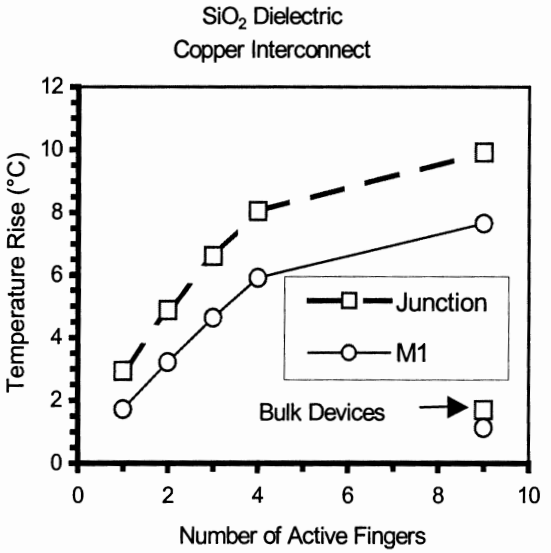

Figure 4. Effect of multiple active fingers on Junction and M1 temperature rise.

With multiple fingers active, the junction temperature rise increases as shown in Figure 4 even though the heat dissipation per unit channel width remains the same (0.06 mW/μm). Because of the close thermal coupling between fingers within the same body, our results clearly show that the junction-to-chip thermal resistance increases by more than a factor of three as more fingers become active. These results show that the conventional use of a single thermal resistance in SPICE type models for a SOI device without differentiating between a single-finger or a multi-finger structure is erroneous, in particular, the use of a thermal resistance value derived or measured from a single-finger isolated device would fail to properly account for the temperature rise of multi-finger devices due to self-heating. Also the SPICE models can not account for both types of geometries simultaneously for thermal calculations. By comparison, the temperature rise in a similar bulk device is small (Fig. 4) and the circuit simulation errors are negligible.

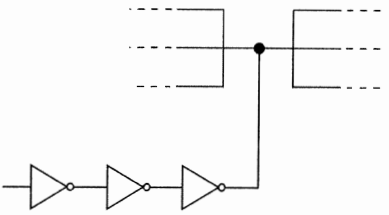

Figure 5. Clock tree used for performance analysis.

Circuit performance was evaluated using the clock tree from a real microprocessor shown in Figure 5.

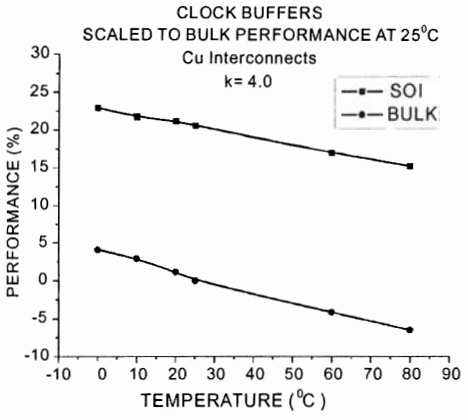

Figure 6. Performance v/s temperature for SOI and bulk clock buffer.

Performance changes with respect to the bulk CMOS performance at 25°C for SOI and bulk devices at a dielectric constant of 4.0 are shown in Fig. 6. For the chosen *Leff* and VDD (1.8 V) the performance gain is over 20% for SOI in the temperature range of 30 - 80 °C and reduces at lower temperatures. The performance change for SOI and bulk per 10 °C change in junction temperature is 1.2% and 1.32% respectively. Also the increased temperature adds to the degradation in reliability of SOI (not shown here).

4. Conclusions

1. 3-D thermal analysis shows significant coupling between adjacent fingers of multi-finger SOI devices. The junction temperature rise in multi-finger devices was a factor of three higher than predicted by 1-D thermal resistance models of single finger devices. 2. Junction temperature rise in SOI due to self-heating in high power devices like clock buffers can be 10 °C. Conduction from the channel can raise the M1 temperature 10 °C above that of the silicon. 3. Increase in temperature degrades the performance incrementally.

References:

1. Su, Lisa T. et. al., IEEE Transactions on Electron Devices, Vol. 41, No. 1, Jan 1994, pp. 69-75.
2. Workman, Glen O. et. al., IEEE Transactions on Electron Devices, Vol. 45, No. 1, Jan 1998, pp.125-133.