A Simulation Evaluation of 100nm CMOS Device Performance

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Abstract

This paper presents a simulation evaluation of the performance of 100nm MOSFET devices. Calibration of 2D physical device models against measured 0.13 micron NMOS and PMOS devices forms the basis for a study of different MOSFET device options. The sensitivity of individual design factors is assessed on the device Ion/Ioff performance. The feasibility of achieving the ITRS-2000 specifications is addressed and limitations to the benefit of gate dielectric thickness scaling are identified.

1 Introduction

The continued applicability of 2D drift-diffusion transport modelling to MOSFETs, albeit with careful calibration of velocity-field characteristic and transverse field dependence, is a huge benefit to the TCAD support of technology development. Models can be quickly calibrated to a sufficient accuracy and deployed in large-scale simulation studies to provide an initial feasibility analysis and guidance of device design and performance specifications for new CMOS technology generations. This paper presents an evaluation of the Ion/Ioff performance of 100nm MOSFET devices based upon predictive simulation from device models calibrated on 0.13μm CMOS.

2 Models

In this work, models were calibrated to data from 0.13 micron CMOS development with 2.5nm gate dielectric[1]. This included assessment of the doping activation in the gate, as shown in fig. 1, and the mobility model, as shown in fig 2. A parameterised

[1] S Kubicek et al "Investigation of intrinsic transistor performance of advanced CMOS devices with 2.5nm NO gate oxides" Proc IEDM-99 p823 (1999)

MOSFET template was then established in the 2D-device simulator, allowing variation of important doping and geometry variables. These include physical gate dielectric (equivalent SiO_2, EOT) thickness (Tox), gate activation, source/drain extension (MDD) dose and junction depth (X_J), inner spacer (1) and outer spacer (2) widths, channel (VTA) and halo dose, gate length (L_G) and supply voltage (V_{DD}). Design-of-experiments methods were used to evaluate the effects of these variables and to build response-surface models for the device parameters, which were then exported into a spreadsheet tool.

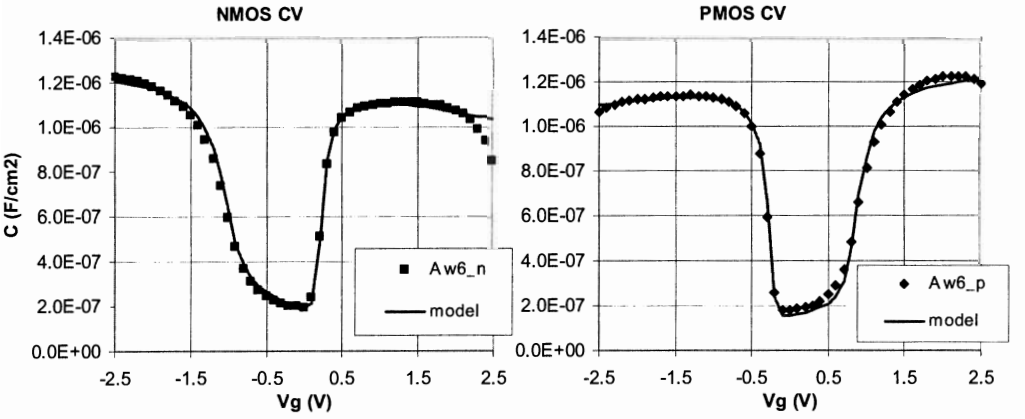

Fig. 1. C(V) for the N+ and P+ gate capacitors comparing model and measurements.

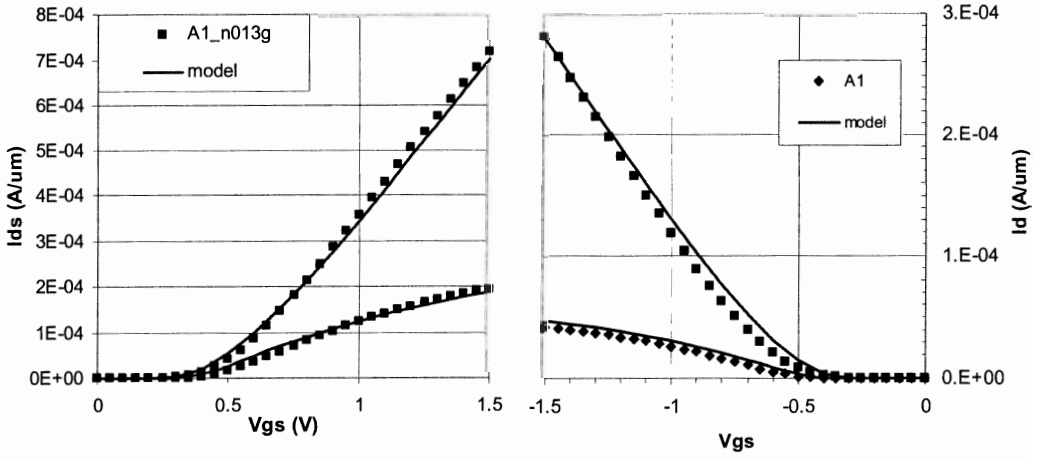

Fig. 2. Id(Vg) plots for 130nm NMOS device at Vds=0.1 and 1.5V comparing calibrated Avant! MEDICI™ model and measurements.

3 Device Sensitivity

The main effects in the on/off current (Ion/Ioff) space are shown as vector plots in fig. 3 for NMOS and PMOS conventional MOSFETs with halo doping to counteract short-channel effects. The centre-point device structure variables are shown and use Tox of 1.85nm. The effect of modifying the channel dose, shown as a dashed line, represents the neutral behaviour of the device (VTA tunes the desired off-current for the technology). Design directions to the right of this line increase performance.

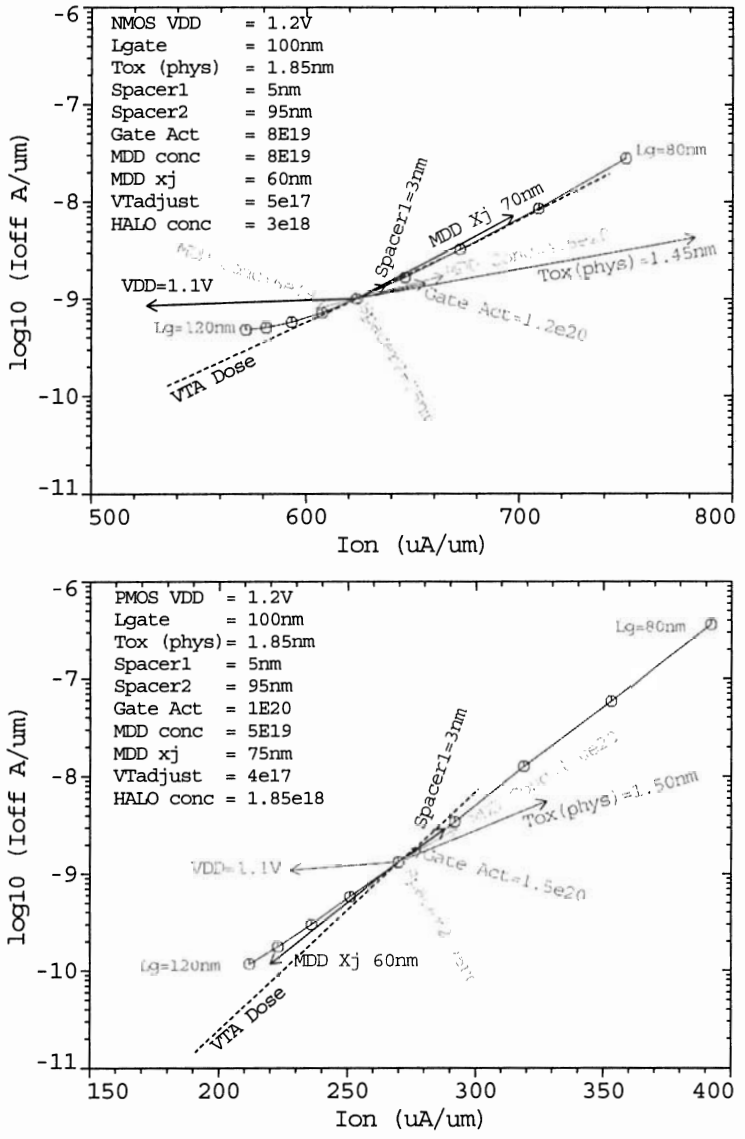

Fig. 3. Effects on Ion/Ioff performance of NMOS (upper) and PMOS (lower). I_{on} = $I_{ds}(@V_{ds}=V_{gs}=V_{DD}, L_G^{nom})$, $I_{off}=I_{ds}(@V_{ds}=V_{DD}, V_{gs}=0, L_G^{nom})$. L_G^{nom} is the nominal gate-length.

The strongest effect is from gate oxide thickness: reducing to 1.45nm gives a 25% increase to the NMOS Ion with only x4 increase in Ioff (assuming that gate leakage is controlled to <1A/cm^2). There are also benefits in increasing the extension and gate doping activation. Interestingly, reducing L_G does not give a strong increase in performance, due to worsening short-channel effects at this X_j: a 15% decrease in L_G gives x9 increase in Ioff. V_{DD} has a significant effect: reducing from 1.2 to 1.1V gives a 16% reduction in Ion. Aggressive scaling of the equivalent gate dielectric thickness leads to a high-field mobility reduction which outweighs the increased gate capacitance, ultimately producing a net degradation in the drive-current normalised to a given off-current (figure 4). For 1.2V the limit is 0.85nm increasing to 1.2nm for low leakage devices.

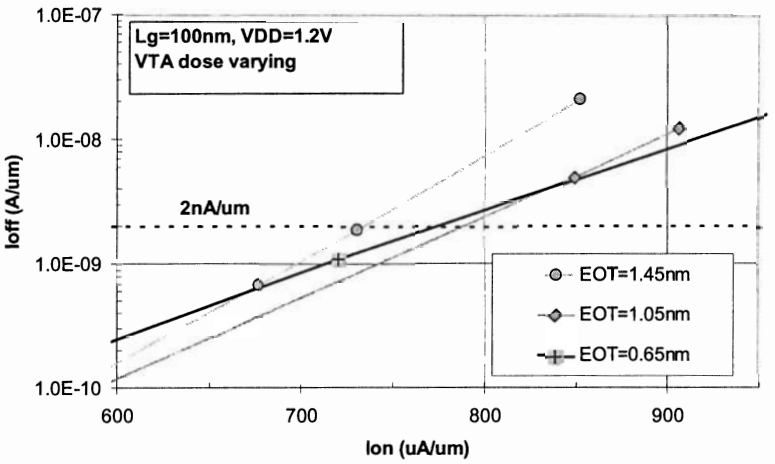

Fig. 4. Predicted I_{on}/I_{off} behaviour of L_G=100nm NMOS devices for different gate dielectric thickness (equivalent SiO_2) at V_{DD}=1.2V. The lines represent the effect of adjusting channel dose. For I_{off} = 2nA/μm, scaling the gate dielectric below 0.85nm gives no benefit.

4 Conclusions

We estimate that the ITRS[2] high performance targets of N/PMOS I_{on}=750/350μA/μm can just be achieved with Tox=1.5nm, V_{DD}=1.2V at I_{off} of 2nA/μm for nominal L_G (100nm), which is x10 lower than the ITRS I_{off} specification at worst-case gate length. The drive-current benefit from future scaling of gate dielectric thickness (and gate length) is compromised by mobility degradation at high fields and high doping.

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[2] ITRS-2000 Update, http://public.itrs.net