Modeling the Impact of Body-to-body Leakage in Partially-Depleted SOI CMOS Technology

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Abstract

We study the impact of body-to-body leakage on the performance of partially-depleted silicon-on-insulator (SOI) CMOS technology using TCAD. The body-to-body leakage could be significant because of aggressive technology scaling as shown by process simulations. A fifteen percent degradation in overall delay time is observed by device and mixed-mode circuit simulations. Numerical junction leakage models for accurate body potential modeling are also discussed.

1. Introduction

As SOI CMOS technology becomes mainstream for high performance applications, accurate and efficient modeling is crucial for successful SOI technology development and optimization [1][2]. In addition to junction capacitance reduction, the elimination of body effects in stacked MOSFET (e.g. NAND) circuits can provide a significant performance advantage in partially depleted (PD) SOI technologies. The two MOSFETs in a stacked configuration usually share a common diffusion. The bodies of these MOSFETs are normally isolated by abutting the common diffusion against the buried oxide. However, as technology scales, both the poly-to-poly spacing and the junction depth are substantially reduced for density reduction and control of short-channel-effects, respectively. A leakage path between the bodies of the MOSFETs could be formed if the common diffusion does not abut the buried oxide due to scaling. In this paper, we evaluate the performance impact in such a situation. A complete TCAD flow from process, device, to circuit (mixed-mode) simulations has been established. We also discuss key numerical leakage models for accurate body potential modeling.

2. Junction Leakage Models

Because of the Vdd scaling and strong halo used in scaled MOSFETs, the body potential in a PD-SOI FET at and below threshold can be well characterized by two back-to-back diodes (see figure 1). The body potential at the off condition can be estimated by the continuity between the forward and reverse diode current. Figure 2 displays a typical diode current characteristic at forward and reverse-biases. Note that it is the balance of leakage current (not the magnitude) that determines the body potential. At high reverse bias, the weaker temperature dependence suggests that leakage is dominated by band-to-band tunneling.

Figure 3 shows that the band-to-band tunneling is mainly located near the halo and extension junction. At low bias, the leakage current is dependent on the trap density related to defects. This leakage can be accurately described by a field-enhanced carrier lifetime model in a SRH-like recombination formulation. However, the defect density is

highly process dependent. The ion-implantation species and its implant energy and rapid thermal anneal (RTA) conditions can substantially affect the defect related leakage current. The defect related current is distributed along the source/body junction as shown in Figure 3. Thus, reducing the junction area can substantially increase the floating body effect.

Diode characteristics from a body-tied SOI MOSFET at different temperatures are needed to separate the defect-related current and the band-to-band tunneling current. Special attention must be paid to ensure diode current is not obscured by the gate induced drain leakage (GIDL). The formulations for junction leakage are derived from Hurkx [3] and Kane [4] and are summarized in Table 1. The models have been successfully used for silicon channel thickness optimization [5].

Table 1: Diode leakage models

Defect related leakage current
$U = \frac{(np - n_i^2)}{\tilde{\tau}_n(n + n_1) + \tilde{\tau}_p(p + p_1)}$ $n_1 = N_C \exp[\frac{E_t - E_C}{kT}], p_1 = N_V \exp[\frac{E_V - E_t}{kT}].$ $\tilde{\tau}_k = \frac{\tau_k(N_D, N_A, T)}{\aleph_k(F,T)}$, $\aleph_k(E,T) = \aleph_k(E,T)_{CL} + \aleph_k(E,T)_{QM}$
Band-to-band tunneling
$G^{BB} = D(\psi, E_{fn}, E_{fp}) \times A \times E^n \times \exp(-B/E)$ $D(\psi, E_{fn}, E_{fp}) = \frac{1}{\exp[(-E_{fp} - q\psi)/kT] + 1} - \frac{1}{\exp[(-E_{fn} - q\psi)/kT] + 1}$ $A = A_0 \times \left[\frac{m_r}{E_g}\right]^{\frac{1}{2}}, m_r = 0.198 \times m_0 \times \frac{m_T}{m_{300}}$ $B = B_0 \times \left[\frac{m_r}{0.198 \times m_0}\right]^{\frac{1}{2}} \times \left[\frac{E_g}{1.1eV}\right]^{1.5}$

3. Impact of Body-to-body Leakage

When the poly-to-poly spacing is scaled with technology, the common diffusion between two SOI MOSFETs in a stacked structure (e.g. NAND gate) can become shallower due to shadowing effects. A schematic device structure is shown in Figure 4. The body potential can be very different depending on whether the common diffusion junction is abutted to the BOX or not. The body potential could be strongly linked when there is a direct body-to-body leakage path. When the two bodies are strongly linked, the potentials in the two bodies are identical. The potential is self-limited by the forward biased diode of transistor (1). The body potential is pinned at around 0.4V. If the two bodies are isolated very well, the body for transistor (2) should be charged up to 1.8V (Vdd) when the gate in transistor (2) is turned "on". The large difference in body potential of transistor (2) can substantially degrade circuit performance. Detailed process simulations using IBM's T-Suprem were used to obtain the junction profile for the common diffusion. A small reduction of the poly-to-poly spacing resulted in a shallower common diffusion due to shadowing effects. The body-to-body leakage is increased which reduces the body potential of transistor (2). The junction capacitance is also increased due to a larger junction area. To

study the body-to-body leakage impact on circuit performance, mixed-mode capability in Fieldday3 [6][7] was used to simulate a SOI two-way NAND-gate circuit. Figure 5 displays the simulated input and output wave forms. More than 10-15% degradation in overall delay time is observed. The absence of the body effect in a NAND gate is one of the performance advantages for SOI. To gain this benefit, body-to-body leakage must be minimized by careful device design. Further scaling of the silicon channel could alleviate this body-to-body leakage problem. In summary, accurate numerical leakage models have been developed and calibrated. The models have been used for body-to-body leakage minimization.

References

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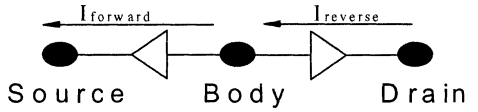

Figure 1: Equivalent circuit model for the floating body potential at and below threshold. The body potential can be determined by balancing the reverse and forward biased diode current.

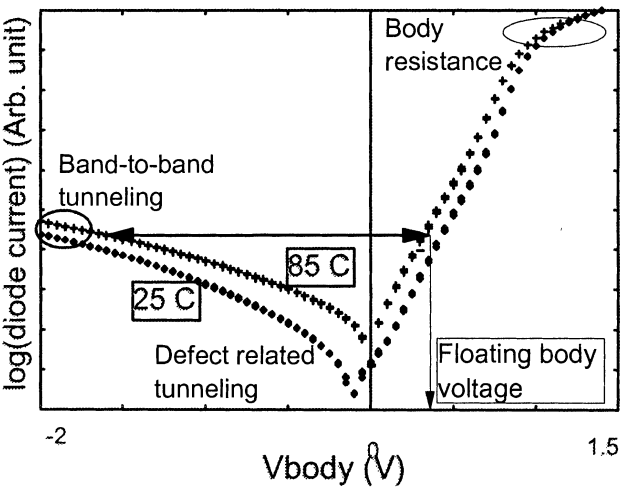

Figure 2: Measured diode leakage current at 25C and 85C. The floating body potential of a scaled PD-SOI MOSFET can be determined by equating the forward and reverse biased diode currents.

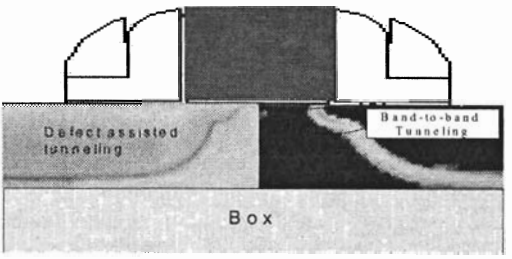

Figure 3: Simulated diode leakage current density at Vds=1.8V, Vs=Vg=0V. The maximum band-to-band tunneling current is located near the drain extension and halo junction. The defect-related current is distributed along the source and body junction.

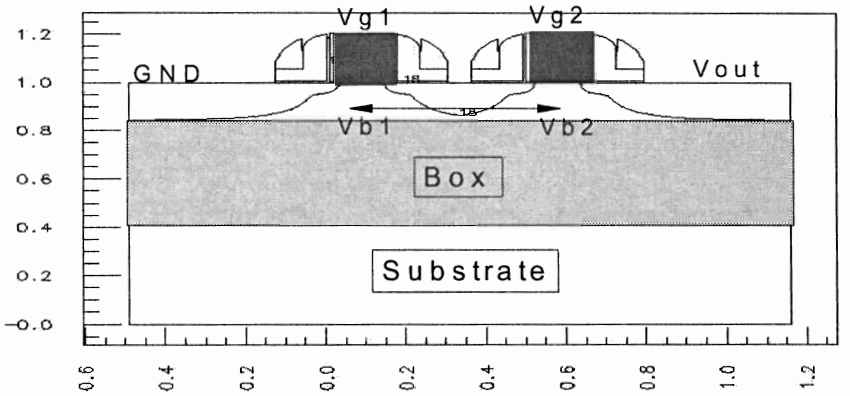

Figure 4: Schematic device structure and terminal voltages definition.

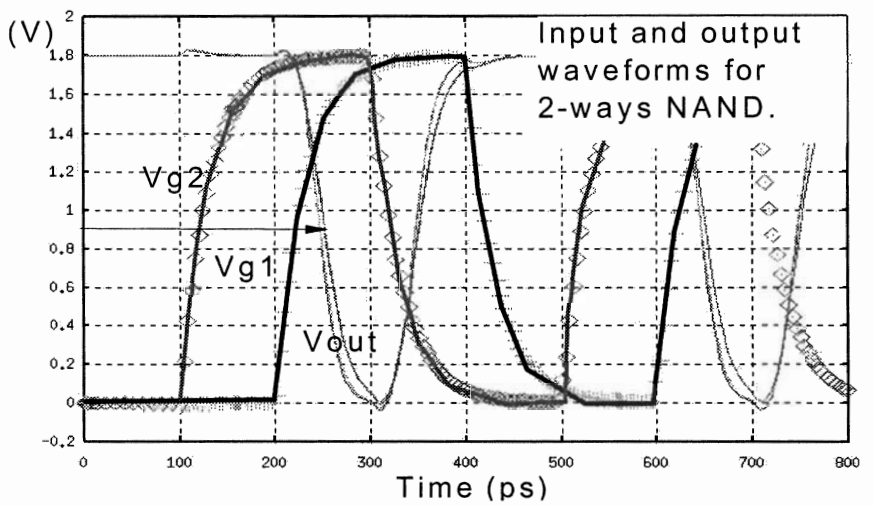

Figure 5: Mixed-mode simulation comparing strongly body-linked and weakly body-linked NAND gate on a 0.25 um SOI CMOS technology. The strongly body-linked NAND gate is about 10-15% slower.