Electrothermal Device Simulation of an ESD Protection Structure Based on Bipolar DC Characteristics

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Abstract

The high current characteristics of an ESD protection structure fabricated in a smart power technology is calculated by the use of electrothermal device simulation. We find reasonable agreement with experimental results after careful calibration of the technology-dependent transport parameters. The still existing differences between measurement and simulation results are discussed, together with some conclusions for the application of our simulation strategy in future.

1 Introduction

Nowadays ESD protection structures are conceived as a must in view of the high reliability requirements of integrated circuits. Several protection principles are known and widely used [1]. However, the development of devices matching the protection needs for a given technology and application field still relies mostly on expensive and time-consuming experiments. One of the reasons is that numerical simulations are based on physical model parameters which require a very careful calibration for the consistent and reliable modeling and prediction of high current characteristics of protection devices. In this paper we demonstrate the simulation of an ESD protection structure fabricated by means of an industrial

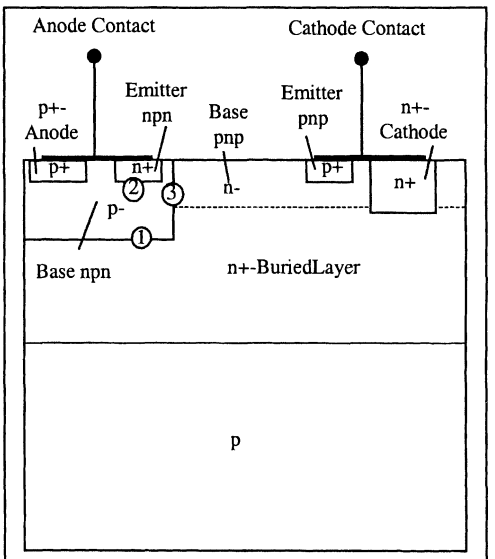

Fig. 1 Schematic view of the ESD protection structure investigated

smart power technology. The physical parameters are extracted by comparing DC measurements with isothermal simulations of DC characteristics. Yet, also the transient high current behavior is reasonably reproduced using these parameters.
A schematic view of the device under investigation is drawn in Fig. 1. The anode contact is assumed to be at ground potential during ESD stress, while the cathode contact is connected to the discharge path. The discharge through the device forces the cathode voltage to rise rapidly, thus driving junction 1 into avalanche breakdown. As a consequence of the strong increase of the hole density in the p^--base, junction 2 gets forward-biased, allowing the vertical npn-transistor (with the n^+-buried layer as collector) to drive an increasing amount of the device current. The cathode voltage is reduced drastically with increasing transistor current. This snap-back behavior is observed until the terminal voltage attains its minimum value (holding voltage V_H). The lateral pnp-transistor also conducts part of the current, and, thus aids to further reducing the terminal voltage. Once V_H is reached, the terminal voltage rises again with increasing current due to high injection.

2 Transport Parameters of the Simulation Model

The simulations were performed using the commercial device simulator DESSIS. Two devices were selected for calibration: a quasi-1D reverse-biased pn-diode and a cylindrical npn-bipolar transistor operated in active mode. Both device types play a fundamental role in the function of the full protection structure, as explained in section 1.
The breakdown voltage V_{BD} of the pn-diode was measured for 233K, 298K and 423K, in order to adjust the coefficients controlling the temperature dependence of the impact ionization coefficients according to Chynoweth's law (see e.g. [3]). After calibration, the simulations conform well to the experiment, as it is shown in Table 1.
The transistor characteristics $I_c(V_e)$ and $I_b(V_e)$ as well as the current gain $\beta(I_c)$ were measured at room temperature with base and collector at fixed potentials and varying emitter voltage V_e. Low current conditions (small V_e) in the base and collector current characteristics were used to calibrate the lifetimes in the Schockley-Read-Hall-model and the carrier mobilities (see Fig. 2). For high current conditions (large V_e) the static current gain $\beta=I_c/I_b$, shown in Fig. 3 as a function of collector current I_c, is correctly reproduced after calibration of the model parameters for trap-assisted- and band-band-Auger recombination, and for bandgap narrowing. The latter quantities have a very sensitive influence on the device characteristics because of the exponential dependence of the carrier concentrations on the bandgap energy. Proper adjustment of these parameters yield excellent agreement of the simulation results with the measured data (Fig. 3.).

Table 1 Comparison between measured and simulated breakdown voltages

T	*233K*	*298K*	*423K*
V_{BD}, *measured*	41,1	43,6	47,1
V_{BD}, *simulated*	43	44	47

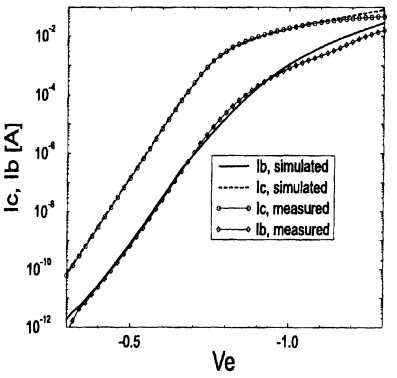

Fig. 2 Collector and base current vs. emitter voltage for the bipolar transistor

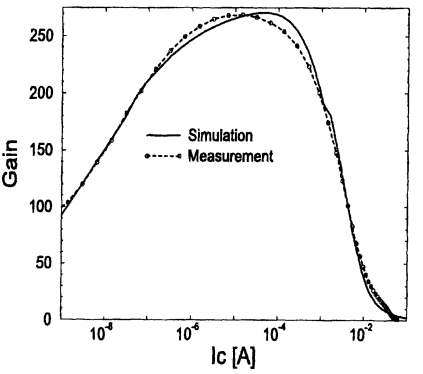

Fig. 3 Current gain vs. collector current for the bipolar transistor

3 Measurement and Simulation of High Current Characteristics

Experimentally, the I-V-curve is determined by forcing rectangular current pulses through the device, with varying current height but fixed duration of 100ns (transmission line pulse, TLP). For a given current, the voltage measured between the terminals is averaged, thus defining one point of the high current characteristics.
For the simulation of these measurements, the current pulse through the device is simulated using the drift-diffusion approach extended by the heat transport equation, in order to account for the self-heating of the device. Fig. 4 shows the calculated high current characteristics. The simulated holding voltage of 30V is significantly larger than the experimental value of 22 V.
Two 'hot spots' are observed in the simulation, which are located near the base-collector junction of both the npn- and pnp-transistors (junctions 1 and 3 in Fig.1). The maximum temperature is 585 K at a current level of 1 A.

4 Discussion

Compared to the calibration strategy pursued in [4] and [5], we followed a more comprehensive approach by also using the IV characteristics and current gain of the npn bipolar transistor for calibration. But, compared to those results, the agreement of TLP simulations and measurements is not as good. The breakdown voltage comes out correctly in the simulation, while the holding voltage is overestimated, as can be concluded from Fig. 4. Since the ESD protection device is primarily operated as a bipolar transistor in the high current range, and the simulation had been successfully calibrated with reference to such a device, one should have expected a better agreement.
The simulation of the current pulses also reveals that the lattice temperature rises up to 585K inside the device at 1 A. As the calibration was performed for room temperature, the temperature dependence of the physical parameters is possibly not correctly incorporated in the models used. When the npn-transistor reaches the high-injection regime, the free carriers in the space-charge region (SCR) at the collector-

base junction cannot be neglected anymore. Considering the npn-transistor in only one dimension, the collector current density can then be calculated by means of

$$j_C = \mu_e \cdot n_C \cdot E_C , \qquad (1)$$

while for the emitter current density,

$$j_E = \frac{2 \cdot q \cdot D_a \cdot n_i}{W_B} \cdot \exp\left(\frac{V_{BE}}{2 \cdot k \cdot T/q}\right) \qquad (2)$$

holds if $W_B \ll L_a$ (see e.g. [2]). Here D_a and L_a denote the ambipolar diffusion coefficient and diffusion length, E_C and n_C are electric field and electron density in the collector-base SCR, respectively, and W_B is the effective base width).

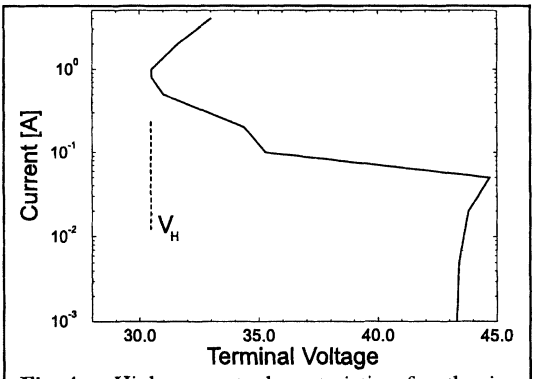

Fig. 4 High current characteristics for the investigated device. The simulated holding voltage V_H is indicated.

These equations reveal that a number of transport parameters account for the overall device behavior, and that the local device temperature, as well as manufacturing processes like implantation and annealing (influencing e.g. the recombination rates) may cause strong variations of those parameters in space and time. This is why careful calibration of all model parameters is so important to get the possibility of predictive device simulation.

Our results show that the behavior of ESD-structures in the high current regime cannot be represented by two separated devices, namely a reverse biased diode and an operated BJT. The observed discrepancies have to be investigated in more detail to identify their origin and to develop test structures for the extraction of the relevant model parameters. These investigations have to include the temperature dependence of the relevant model parameters up to the temperatures that arise in these devices under high current stress conditions.

References

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