Advanced Hybrid Cellular Based Approach for Three-Dimensional Etching and Deposition Simulation

A. Hössinger, T. Binder, W. Pyka, and S. Selberherr

Institute for Microelectronics, TU Vienna, Gusshausstrasse 27–29, A-1040 Vienna, Austria
Phone: +43-1-58801/36027, Fax: +43-1-58801/36099 Email: Hoessinger@iue.tuwien.ac.at

Abstract

For the simulation of etching and deposition processes the cellular method is very popular, because of its high robustness compared to alternative methods like the level set or the moving boundary approach. We present a method for the simulation of topography processes based on the cellular method that overcomes the problem of loss of information when using a cellular based simulator in combination with simulators using polygonal data representations. Additionally the new method allows to increase the resolution of the topography simulator without a significantly higher memory requirement.

1 Introduction

For three-dimensional simulation of etching and deposition processes cellular based algorithms [1] [2] have advantages to polygonal based algorithms and level set algorithms due to their high robustness. For instance the formation of voids which is a very serious problem for polygonal based algorithms is implicitly handled. Nevertheless the major drawback of the cellular based simulators is the cellular data format. On the one hand side the cellular resolution is not very high because the memory requirement increases dramatically by choosing a higher accuracy. But when a topography simulator is applied to front end process simulation also thin layers like the gate oxide in a MOS transistor have to be resolved accurately. This means that the cell size should be smaller than one tenth of the gate oxide thickness. For instance, if the volume of the simulation domain is 1 μm^3 and the gate oxide thickness is 5 nm 8 billon cells were necessary to discretize the simulation domain, while the error is still not less than 10%.

A way to reduce the memory requirement is to use more advanced discretization methods than a simple regular grid. A bucket octree based representation could be the method of choice, but it still suffers from the fact that the discrete representation is normally not compatible to the polygonal based data format of other simulators used for semiconductor process simulation. As a consequence, several conversions between the cellular and the polygonal data format are necessary, if the cellular based simulator is integrated into a process flow. Errors of the order of the resolution of the cellular representation are introduced by each conversion. As already mentioned, small structures (especially thin layers) present in the simulation domain may be seriously modified or even get lost in the worst case, although for instance, not even small modifications of the gate oxide thickness are tolerable.

We present an advanced hybrid cellular approach which attacks the discretization error problem from two sides. On the one hand side we avoid a discretization of the complete simulation domain by restricting the descritization to a layer around the surface attacked by the topography process and on the other hand side two levels of cell resolution are used. Both measures give a higher cellular resolution resulting in a smaller discretization error.

2 Internal Data Representations

During the simulation two internal data representations are used. The core of the topography simulator is based on a regular grid layed over the whole simulation domain. Each cell defined by this grid either can contain material information or another regular grid defining refined cells. Note that no physical memory is associated with this grid at the beginning. Just during the simulation the material information is generated and stored on grid cells.

The topology of the complete simulation domain is stored seperately in the so called Wafer State Server [3]. This Wafer State Server holds the structure of the simulation geometry in a thetrahedral volume mesh discretized format and provides functions to comfortably access information about the simulation domain. Thereby material cells used by the topography simulator can be easily generated during the simulation. To achieve an accaptable access time the mesh is stored on a finite octree inside the Wafer State Server.

3 Topography Process

First the upper surface (surface attacked by the topography process) of the simulation domain is extracted by the Wafer State Server and discretized pointwise. Around each discretized point, refined topography simulator cells (called refined cell in the following) are generated. The material type of the cells is determined by the Wafer State Server and as a consequence the size of the structuring element [2] related to each cell placed at a material interface.

After setting up the discretized surface the topography process is performed. Thereby all previously determined structuring elements are applied to the simulation domain. All cells covered by the smallest rectangular prisms containing the structuring elements are defined at that time. Defining a cell means that memory is allocated for the cell if necessary and all the informantion stored on the cell is prepared by the Wafer State Server. This procedure is indicated by the gray area in Fig. 1. All cells containing the surface, the front of the topography process and interfaces between different materials are additionally refined (as indicated for the surface cells in Fig. 1) to further increase the resolution in such sensitive areas.

The simulation proceeds similar as in the classical cellular approach, meaning that the material type of all cells attacked by the topography process is changed during the simulation. The only differences to the classical approach are that

- memory is successively allocated whenever a cell is attacked outside of an allocated memory area.
- cells close to the process front (e.g. etch front) become refined cells.
- cells moving away from the process front are converted back to simple cells if they contain refined cells just of one material type.

The use of a two level cell resolution does not only save memory but also increases the performance of the simulation, because generally each cell has to be checked whether it is inside or outside of a structuring element in order to determine if the material type of a cell has to be changed. If a cell which is not refined is completely contained within or outside of the structuring element, its subcells need not to be checked. This significantly reduces the number of test operations, if the size of the unrefined cells is smaller than the size of the structuring element.

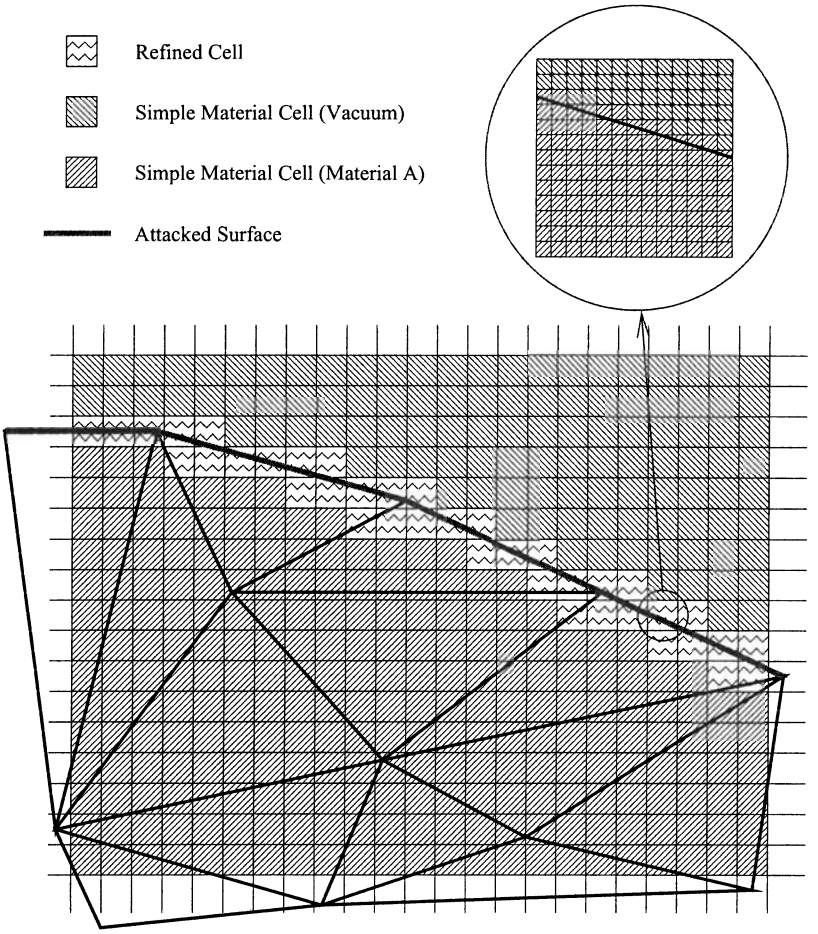

Fig. 1: Illustration of the descretization procedure.

4 Post Processing

After completing the topography simulation the topology of the modified simulation domain has to be generated. Therefore a triangulated representation of the etchfront is determined from the cellular data structure, simply by generating two triangles from all interfaces between a material cell and vacuum cells. Since all cells around the front of the topography process are refined cells just triangles with half the area of one side of a refined cell are generated. In order to reduce the huge number of triangles and to improve the quality of the triangulated front two postprocessing routines are applied.

On the one hand side the manhatten like structure is smoothed by projecting each point into a plane with the minimum distance from points surrounding the point which has to be projected. By restricting the offset due to projection to the half length of the diagonal of a refined cell the generation of illegal structures (intersecting triangles) is avoided. Thereby the angle between triangles which should be coplanar is made quite small.

On the other hand side the number of triangles is reduced by removing edges [4] which are surrounded just by approximately coplanar triangles (the angle between the triangles is below a minimum tolerable angle). The number of triangles is usually significantly

reduced and, additionally, more vestiges of the manhatten like structure are removed.

Finally a new wafer has to be set up which contains all the information available before the topography process, modified just by the effects of the topography process. At that point the major advantage of coupling the topgraphy simulator with the Wafer State Server shows up. During the simulation the Wafer State Server keeps track of mesh element attacked by the topography process. Thereby the Wafer State Server finally knows which segments have been attacked by the topography simulation and just these segments are modified. The modification is performed by constructing new segments from the old ones by cutting the segment surfaces with the etch front and remeshing the resulting topography. This procedure is schematically depicted in Fig. 2. In case of a deposition simulation no existing segments have to be modified. Just new segments are created by meshing the space between the initial wafer surface and the final deposition fronts. Worth mentioning is that more than one front may have been generated during the simulation due to the formation of voids.

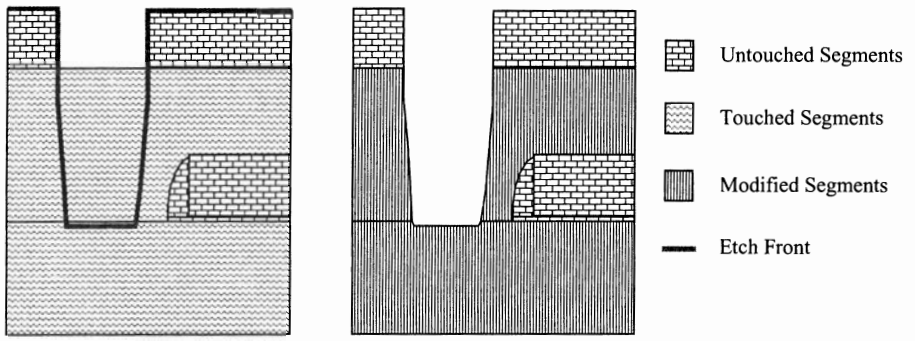

Fig. 2: Illustration of the modification of the wafer state data due to the etch process.

5 Conclusion

We have presented a method for the simulation of etching and deposition processes which makes use of the robust cellular algorithm. The new method overcomes the problem of conversion errors when a cellular based simulator interacts with simulators based on polygonal data structures. Additionally the memory requirement is drastically reduced so that also large structures can be simulated with sufficiently high resolution.

Acknowledgment

This work is supported by LSI Logic and by APART (Austrian Program for Advanced Research and Technology) from the Österreichische Akademie der Wissenschaften.

[1] W. Pyka, R. Martins, and S. Selberherr, "Optimized Algorithms for Three-Dimensional Cellular Topography Simulation," *IEEE J.Technology Computer Aided Design*, 2000. `http://www.ieee.org/products/online/journal/tcad/accepted/Pyka-March00/`.

[2] E. Strasser and S. Selberherr, "Algorithms and Models for Cellular Based Topography Simulation," *IEEE Trans.Computer-Aided Design*, vol. 14, no. 9, pp. 1104–1114, 1995.

[3] T. Binder and S. Selberherr, "Object-Oriented Wafer-State Services," in *14th European Simulation Multiconference* (R. V. Landeghem, ed.), (Ghent, Belgium), pp. 360–364, Society for Computer Simulation International, May 2000.

[4] P. Lindstrom and G. Turk", "Fast and Memory Efficient Polygonal Simplification," in *Proceedings of IEEE Visualization*, vol. 98, pp. 279–286, 1998.