Impact of Substrate Resistance on Drain Current Noise in MOSFETs

Jung-Suk Goo, Simona Donati†, Chang-Hoon Choi, Zhiping Yu,
Thomas H. Lee, and Robert W. Dutton
Center for Integrated Systems, Stanford University, Stanford, CA, USA
goojs@gloworm.stanford.edu
†Dipartimento di Elettronica, Politecnico Di Torino, Torino, Italy

Abstract

This paper identifies the physical origin and contribution mechanism of substrate induced channel thermal noise in MOSFETs. Resistance of the substrate generates potential fluctuations that in turn produce additive channel noise via the channel depletion capacitor. The additive noise may result in a frequency dependence of the drain current noise due to a pole associated with the R_{sub}-C_{depl} network. Its bias and length dependencies conforms to those of reported excess noise, it thus may exaggerate the amount of the channel thermal noise factor.

1 Introduction

It has been known that short channel MOSFETs yield larger drain current noise (S_{i_d}) [1] than the value predicted by the van der Ziel model, which agrees with long channel MOSFETs. However, the amount of the increase is still controversial: some studies have demonstrated a substantial increase while other studies have claimed that less than a factor of two increase has been observed for MOSFETs with 0.17μm [2].

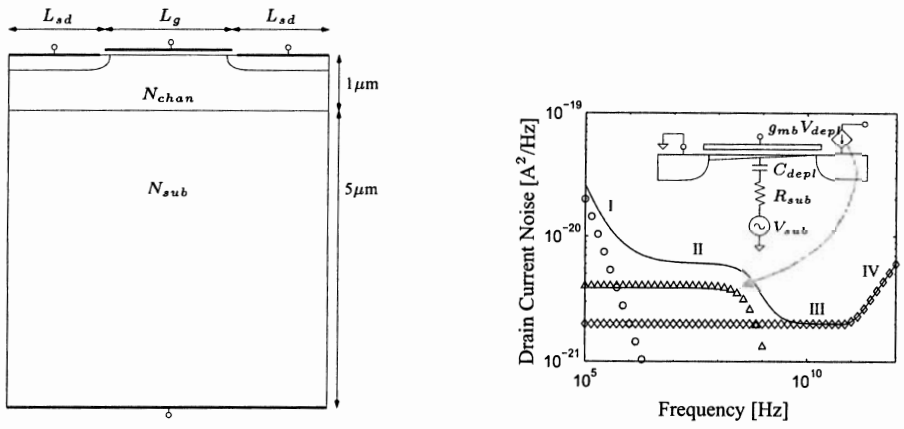
While circuit design commonly assumes that the drain current noise is frequency independent, experimental data has shown a frequency dependence of noise resistance ($R_n \triangleq \frac{S_{i_d}}{4kT|Y_{21}|^2}$) that directly represents the drain current noise in MOSFETs, in the GHz frequency range [3], [4]. However, it has been totally ignored or attributed to measurement errors [4]. This paper investigates the physical origin of the frequency dependence for drain current noise, using physically-based two-dimensional noise simulations. Implications on noise modeling are also discussed.

2 Noise Simulation

In this work, the IFM (Impedance Field Method) is implemented in a general-purpose multi-dimensional device simulator called PADRE [5]. Since the primary interest of the present work is the substrate induced thermal noise, the drift-diffusion model is used and other noise sources, such as $1/f$ noise and generation-recombination noise, are ignored. The MOSFET structure used for noise simulation is illustrated in Fig. 1 (a). This structure, while quite simple, still provides useful analysis results and physical insights. To minimize secondary effects, the junction length (L_{sd}) is reduced.

3 Drain Current Noise Model

It has been a common assumption that the drain current noise only exhibits the $1/f$ noise ($S_{i_d,1/f}$) and white channel thermal noise ($S_{i_d,channel}$) contributions; they dominate regions I and III in Fig. 1 (b), respectively. Although local noise sources generate white noise up to the quantum limit, as frequency becomes much higher than the cutoff



(a) (b)

Fig. 1. (a) Cross-section of the MOSFET structure used for simulation. (b) Anticipated general drain current noise power spectrum for bulk MOSFETs. The solid line is total noise power, the circle symbol is the $1/f$ noise component ($S_{i_d,1/f}$), the triangle symbol is the additive component induced by the substrate ($S_{i_d,sub}$), and the diamond symbol is the channel thermal noise component ($S_{i_d,channel}$). The inset circuit diagram explains the contribution mechanism of the substrate thermal noise to the drain current noise.

frequency, the capacitive coupling between the channel and gate makes propagation of local fluctuations stronger, consequently channel thermal noise increases as region IV in Fig. 1 (b) [6].

In addition, spreading resistance (R_{sub}) of the substrate generates thermal fluctuations given by:

$$S_{v_{sub}} = 4kTR_{sub} \tag{1}$$

where k is Boltzmann's constant and T is the lattice temperature [7]. These fluctuations in the substrate potential modulate the channel charge of the depletion capacitor (C_{depl}) and subsequently produce additive channel noise ($S_{i_d,sub}$), amplified by substrate transconductance (g_{mb}). Since the $R_{sub}C_{depl}$ network in Fig. 1 (b) is a low-pass filter, the amount of additive channel noise is given by

$$S_{i_d,sub} = \frac{4kTR_{sub}g_{mb}^2}{1+(\omega R_{sub}C_{depl})^2} \tag{2}$$

This equation suggests that $S_{i_d,sub}$ has a low frequency noise plateau ($4kTR_{sub}g_{mb}^2$) dominating region II in Fig. 1 (b) and a pole at $f = (2\pi R_{sub}C_{depl})^{-1}$. Thus $S_{i_d,sub}$ effectively increases the drain current noise factor ($\gamma \triangleq \frac{S_{i_d}}{4kTg_{d0}}$). This phenomenon was first discussed by Jindal [7] but only the low frequency noise plateau was considered. For SOI MOSFETs, Faccio *et al.* [8] has introduced a parallel shunting capacitor, which is the sum of the capacitances of the front gate oxide (C_{ox}) and buried oxide (C_{BOx}).

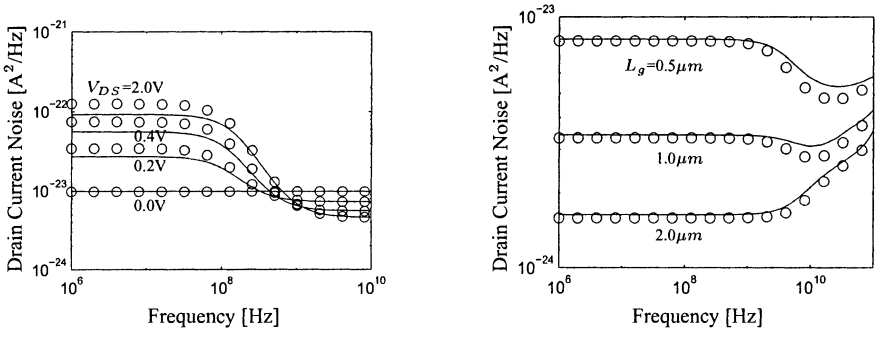


Fig. 2. Simulation results of drain current noise power spectrum. The gate oxide thickness is 60nm, N_{chan} is $5.0\times10^{17}\text{cm}^{-3}$, L_{sd} is 0.01μm, and V_{GS} is 1.5V. The symbols are PADRE simulation results and lines are calculated using (2). (a) A 0.5μm MOSFET for different drain bias conditions. N_{sub} is $1.0\times10^{15}\text{cm}^{-3}$. (b) MOSFETs with different gate lengths. N_{sub} is $3.2\times10^{16}\text{cm}^{-3}$, and V_{DS} is 2.5V.

For bulk MOSFETs, using similar physical reasoning, Kishore *et al.* [3] have explained the phenomenon by adding an RC network between the gate and substrate. However, the channel charge shields the substrate network from the gate electrode under strong inversion conditions. Therefore C_{ox} must be replaced with C_{depl}.

4 Results and Discussions

In Fig. 2 (a) and (b), noise spectra are reproduced by adding the additive component, calculated by using (2), to the simulation results for MOSFETs with a highly doped substrate ($N_{sub} = N_{chan}$). The calculated spectra fit the low frequency noise plateau and pole location, introducing less than 30% error, with C_{depl}-R_{sub}-g_{mb} values extracted from ac and dc simulation results of PADRE. R_{sub} is extracted from a structure without junctions and gate oxide; C_{depl} is approximately equal to $C_{db}+C_{sb}$ if the junction area becomes negligibly small. It is important to note that $S_{v_{sub}}$ indirectly contributes to S_{i_d} via the channel depletion capacitor. Due to the bias dependence of g_{mb}, $S_{i_d,sub}$ is zero under zero drain bias, increases as drain bias increases, and finally saturates for higher drain bias, as shown in Fig. 2 (a). It also largely increases the drain noise factor at low gate bias conditions. Moreover $S_{i_d,sub}$ becomes more significant as the channel length decreases in Fig. 2 (b) since $S_{i_d,sub}$ is proportional to g_{mb}^2 while $S_{i_d,channel}$ is proportional to g_m. Interestingly, these tendencies conform with the reported description of excess drain current noise in short channel MOSFETs [1].

It is worth mentioning that those studies reporting a substantial increase of the drain noise factor have collected data at frequencies below 100MHz due to the bandwidth limits of the transimpedance amplifier. Moreover the samples used relatively primitive technologies, that employ only shallow threshold adjustment doping on a highly resistive substrate. Therefore, it is now suggested that the amount of channel thermal noise has been exaggerated due to the additive thermal noise contribution from the substrate. Thus to characterize the pure channel thermal noise, data needs to be obtained either in

region III or from MOSFETs with a highly doped substrate.

As the transition between regions II and III approaches the GHz range in modern bulk CMOS technologies, modeling using a single RC lump may not be successful. The actual $S_{i_d,sub}$ spectrum is the sum of multiple components with different poles due to the three-dimensional distributed effect of the substrate network; the slope of the transition is much smoother than -20dB/decade, typically below -5dB/decade. Thus prediction of the $S_{i_d,sub}$ characteristic poses an ongoing challenge. Nonetheless, the use of three-dimensional TCAD simulations can be expected to provide additional data in support of new compact modeling.

5 Conclusion

This paper investigates the physical origin, controlling mechanism, and modeling implications of substrate induced channel thermal noise in MOSFETs. Resistance of the substrate generates potential fluctuations that in turn produce additive channel noise by modulating the inversion charge via the channel depletion capacitor. For low-doped substrates, the additive noise may result in a frequency dependence of the drain current noise due to a pole associated with the R_{sub}-C_{depl} network. Since it conforms to the tendency of the reported excess noise, it may exaggerate the value being reported for the channel thermal noise factor. Hence, careful characterization is required to achieve accurate modeling.

Acknowledgments

The authors would like to thank Dr. Mark R. Pinto, Dr. Conor Rafferty, and Dr. Muhammad A. Alam of Agere Systems for providing PADRE. Special thanks go to Texas Instruments for mentoring and promoting this work as a customized SRC project.

References

[1] R. P. Jindal, "Hot-Electron Effects on Channel Thermal Noise in Fine-Line NMOS Field-Effect Transistor," *IEEE Transactions on Electron Devices*, vol. 33, no. 9, pp. 1395–1397, Sept. 1986.

[2] A. J. Scholten, H. J. Tromp, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, P. W. H. de Vreede, R. F. M. Roes, P. H. Woerlee, A. H. Montree, and D. B. M. Klaassen, "Accurate Thermal Noise Model for Deep-Submicron CMOS," in *Technical Digest of IEDM (International Electron Devices Meeting)*, Washington, DC, Dec. 1999, pp. 155–158.

[3] S. V. Kishore, G. Chang, G. Asmanis, C. Hull, and F. Stubbe, "Substrate-Induced High-Frequency Noise in Deep Sub-Micron MOSFETs for RF Applications," in *Proceedings of IEEE CICC (Custom Integrated Circuits Conference)*, San Diego, CA, May 1999, pp. 365–368.

[4] J. J. Ou, X. Jin, C. Hu, and P. R. Gray, "Submicron CMOS thermal noise modeling from an RF perspective," in *Proceedings of the Symposium on VLSI Technology*, Kyoto, Japan, June 1999, pp. 151–152.

[5] S. Donati, M. A. Alam, K. S. Krisch, S. Martin, M. R. Pinto, H. H. Vuong, F. Bonani, and G. Ghione, "Physics-Based RF Noise Modeling of Submicron MOSFETs," in *Technical Digest of IEDM (International Electron Devices Meeting)*, San Francisco, CA, Dec. 1998, pp. 81–84.

[6] J.-S. Goo, C.-H. Choi, F. Danneville, E. Morifuji, H. S. Momose, Z. Yu, H. Iwai, T. H. Lee, and R. W. Dutton, "An Accurate and Efficient High Frequency Noise Simulation Technique for Deep Submicron MOSFETs," *IEEE Transactions on Electron Devices*, vol. 47, no. 12, pp. 2410–2419, Dec. 2000.

[7] R. P. Jindal, "Distributed Substrate Resistance Noise in Fine-Line NMOS Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 32, no. 11, pp. 2450–2453, Nov. 1985.

[8] F. Faccio, F. Anghinolfi, E. H. M. Heijne, P. Jarron, and S. Cristoloveanu, "Noise Contribution of the Body Resistance in Partially-Depleted SOI MOSFET's," *IEEE Transactions on Electron Devices*, vol. 45, no. 5, pp. 1033–1038, May 1998.