Compact device model for partially depleted SOI-MOSFETs

---For simulation of transient drain current arising from the floating body effects---

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1 INTRODUCTION

An accurate simulation of integrated circuits consisting of partially depleted (PD) SOI MOSFETs requires a compact MOS model including parasitic phenomena arising from the floating body. Floating body effects include the occurrence of kink in the saturation current and anomalous sub-threshold slope where impact ionization becomes relevant. In addition, the drain current overshoot [1,2] at "switch on" has been reported even in the absence of impact ionization. The drain current overshoot in PD SOI MOSFETs has a significant history dependence: during switching the body potential proportional to the remaining body charge is determined by both carrier generation/recombination in the body and leakage current through the drain/source-to-body junctions.

The aim of this paper is to develop a complete SPICE model including the floating body effects to accurately estimate history dependent gate delay for reducing the risk of inadequate circuit designs.

2 EXPERIMENTAL

Partially depleted NMOS transistors with gate oxide thickness of 5.7 *n*m were fabricated on 150 *n*m Si film on the buried oxide with 400 *n*m thickness. Figure 1 shows a schematic of the apparatus for pulsed time-current measurements for which NMOS transistors with W/L=10/1 (μm) were used. A pulse voltage was applied to the gate of the MOS devices at a given drain voltage of 0.5V. Time dependence of the drain current was derived from the evolution of the voltage across the resistor connected to the drain which was monitored with the oscilloscope. In order to make such pulse measurements on a microsecond time scale possible, we used 1kΩ resistor.

Figure 2(a) shows the time dependence of the measured drain currents after a pulse voltage of 1.0 V was applied to gate electrodes at t=0*sec* for MOSFETs being subjected to different "off" duration. The measurements have been carried out at a drain voltage of 0.5 V. Figure 2(a) demonstrates that the drain current significantly overshoots at "turn-on" of the MOSFETs. This arises from accumulated minority carriers in the body as shown in Fig.3 which give rise to the increase of the bulk potential, resulting in the increase of the drain current due to positive substrate bias effect.

3 SUB-CIRCUIT MODEL FOR FLOATING BODY POTENTIAL

To model the floating body potential which significantly affects the electrical characteristics of PD SOI MOSFETs, a sub-circuit shown in Fig.4 is proposed for the body voltage based on the equations given by

$$\frac{d\Delta Q_b}{dt} = \alpha\left(\sqrt{V_D - \Delta V_b + \phi_{diff}} - \sqrt{\phi_{diff}}\right) - \frac{\Delta Q_b}{\tau} - I_s\left[\exp\left(\frac{q\Delta V_b}{nk_BT}\right)\right] + \sum_i C_{ib}\frac{d(V_i - \Delta V_b)}{dt}$$

$$\Delta Q_b = \sum_i C_{ib}\Delta V_b$$

where ΔQ_b and ΔV_b are excess charge and incremental body potential in the floating body, respectively.

The first two terms of RHS represent the generation current at the drain/source-to-body junction and the recombination current in the body. The following two terms are forward biased PN junction current at the body-to-source and the displacement currents due to capacitive coupling to other electrodes, *i*= source, drain, gate and Si-substrate. The emission coefficient *n* is introduced into the general diode equation covering the recombination current for the forward biased junction at the body-to-source. A compact device model implemented into commercial circuit simulators[3] includes the latter two terms. The first two terms are, however, left untouched so we try to include those terms into a compact device model. In the drain voltage range of our interest, those terms are approximated as

$$\alpha\left(\sqrt{V_D - \Delta V_b + \phi_{diff}} - \sqrt{\phi_{diff}}\right) \approx g_D(V_D - \Delta V_b)$$

$$and \quad \frac{\Delta Q_b}{\tau} = \frac{\sum_i C_{ib}}{\tau}\Delta V_b = g_B\Delta V_b.$$

As shown in Fig.5, the nominal conductance g_D and g_B are substituted by the resistance depending on width of the depletion region. Once the body potential, ΔV_b, is found, the drain current overshoots can be calculated dynamically through an accurate threshold voltage model in the forward body-bias regime.

4 COMPARISON WITH EXPERIMENTAL AND SIMULATION RESULTS

Note that the decay time of the drain current overshoot covers in a quite wide range from several μsec up to 100 *m*sec. There are two physical mechanisms involved: (1) the rapid decay associated with forward biased leakage current at the

body-to-source junction and (2) the slow decay due to the counter-balance of carrier generation at the body-to-drain junction[4] and carrier recombination in the body. Fig.2(b) demonstrates that the device model presented above well predicts floating-body effects resulting from majority carrier charging in the floating body for switching time of 10 μsec up to 100 *m*sec, over four orders of magnitude. Fig.6 shows the normalized peak current as a function of exponential "off" time duration.

REFERENCES

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[2] H.C.Shin et al., IEEE Trans., Electron Devices, ED-43, 318(1996)

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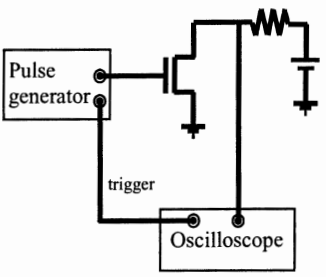

Fig.1 diagram of apparatus

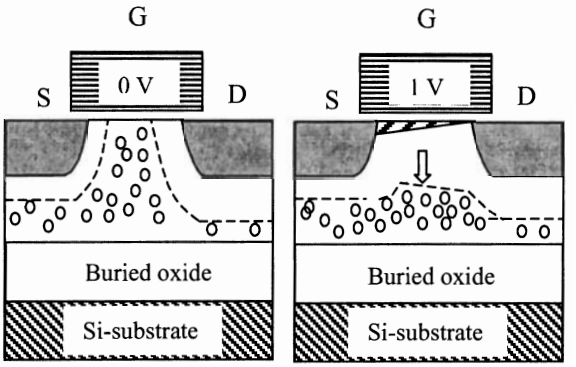

Fig.3. At "switch on", holes near the surface are squeezed into the floating body, leading to positive charged body.

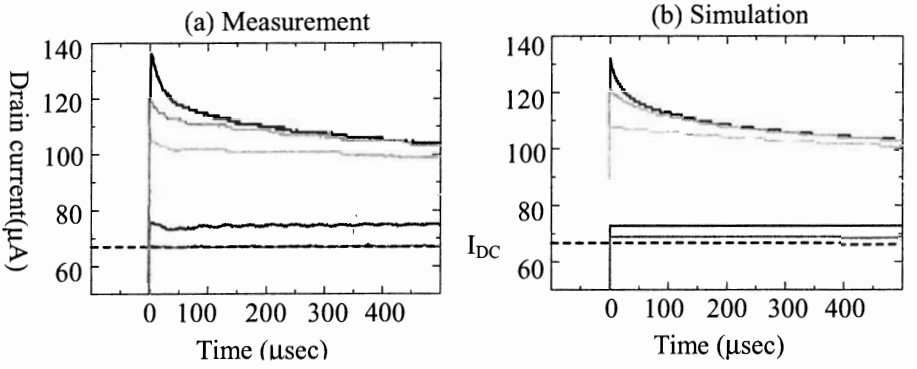

Fig.2. Transient drain current as a parameter "off" duration: t_{off}=10μsec(bottom) to 100msec(top). I_{DC} represents the steady state drain current at DC bias condition.

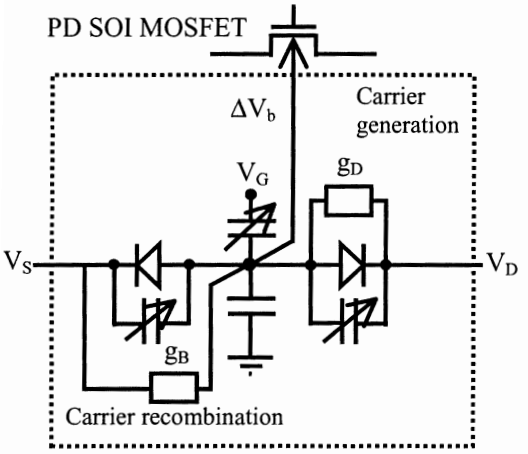

Fig.4. Dashed rectangle: a sub-circuit to track transient behavior of floating body potential, ΔV_d, which controls the threshold voltage of PD SOI MOSFET.

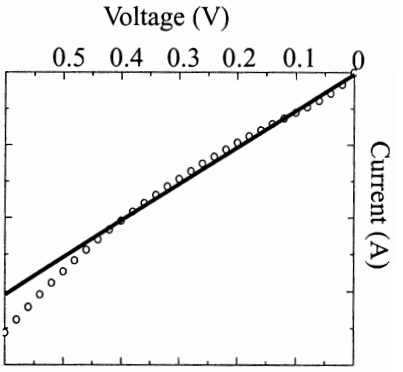

Fig.5. The reverse current characteristic of diode and nominal conductance.

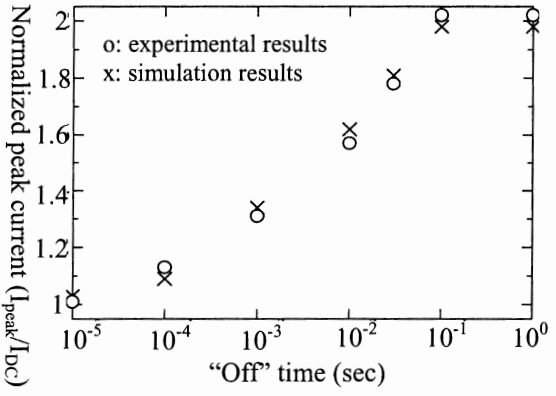

Fig.6. Normalized peak current as a function of "off" duration. Open circles: measured results and Crossed are simulated results

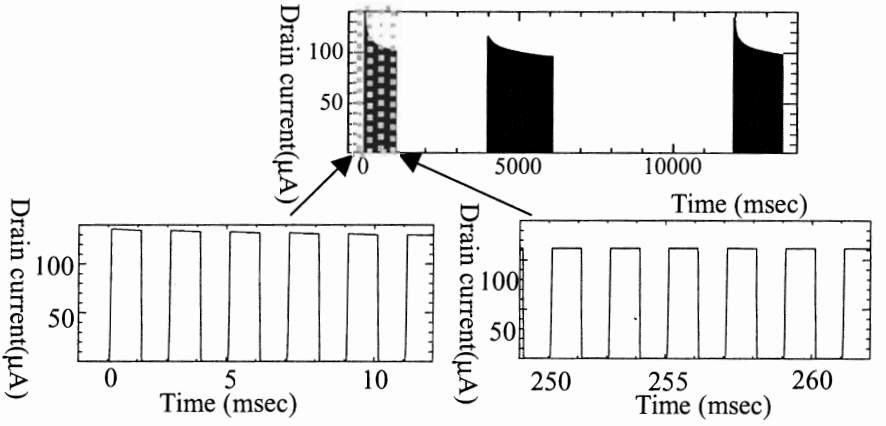

Fig.7. History dependence of drain current under 1msec pulse sequence