Analysis of Ultra Short MOSFETs with High-k Gate Dielectrics

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Abstract

The introduction of alternative gate dielectrics into advanced CMOS devices has quite an impact on the device performance. In this work transient analyses of this type of devices are made for the first time. The analyses are made by mixed-mode simulation of a ring oscillator. It is shown that this method allows a deeper insight into the device properties than mere static analysis. Utilizing the results, first design rules for advanced CMOS devices are extracted.

1 Introduction

According to the International Technology Roadmap for Semiconductors (ITRS) [1], the gate oxide becomes one of the critical issues for short channel devices. If SiO_2 is used the proposed oxide thicknesses are getting smaller than 1nm thus leading to massive direct tunneling from the gate into the substrate. To reduce this parasitic effect alternative materials with higher k values and consequently higher oxide thickness have to be investigated.

2 Analysis of Ultra Short MOSFETs

The first basic analyses of the effects of the increased oxide thickness were carried out in recent years by investigation of the transfer characteristics of CMOS devices [2][3][4]. Basically a degradation of the device performance stemming from an increase of the parasitic capacitances was observed. In this paper these analyses of the device properties are extended to the transient behavior of ultra short devices.

2.1 Transient Simulation Approach

At first a useful criterion that allows the qualification of the transient device properties has to be found. The most interesting quantity concerning the transient behavior of any CMOS circuit is its delay time t_d. The usual definition of the delay time is the time difference between the 50% points of the input and output waveforms [5][6]. This definition should be used with care because the result strongly depends on input waveform and output load [7]. Therefore, the design of the experiment should guarantee a similar waveform to the one expected at actual circuit operation. This can be achieved with a ring oscillator, i.e., an inverter chain with an odd number n of stages, where the output of the last stage is fed back to the input of the first stage. This structure is schematically outlined in Fig. 1.

This circuit will oscillate at a frequency $f = 1/(2nt_d)$. Consequently the delay time reads as $f = 1/(2nf) = t_{osc}/(2n)$, where t_{osc} is the period of the observed oscillation.

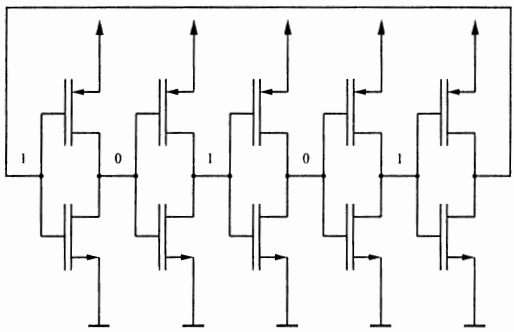

Fig. 1: Ring Oscillator with Five Stages

This experimental setup can be straightforwardly simulated utilizing the mixed-mode capabilities of MINIMOS-NT [8][9]. The ring oscillator used for the calculations is identical to the one outlined in Fig. 1 and consists of an inverter chain with five stages. The PMOS transistor of the inverter was assumed to be symmetric to the NMOS transistor.

2.2 Results

For our research advanced CMOS structures with a gate length of 50nm was chosen. Geometry and doping was chosen according to the ITRS specifications. For our analyses three different high-k device structures, all of them with an equivalent oxide thickness of 0.7nm were used. A device with SiO_2 as gate dielectric was considered as a reference. The high-k structures were chosen with respect to their simplicity in order to make the results as meaningful as possible. Structure I is the simplest of these structures, in which the high-k material completely replaces the SiO_2. Structure II is a device which has a planar high-k layer on top of the Si-substrate outlined in Fig. 2. In Structure III the high-k layer is only under the gate, as shown in Fig. 3. Typically, this structure is processed by removing the gate dielectric and subgate oxide and regrowth of the high-k material.

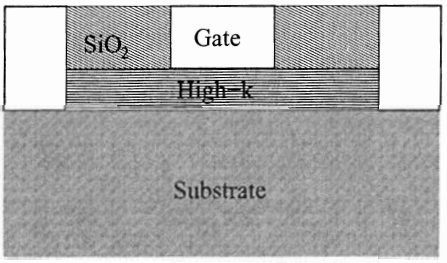

Fig. 2: Structure II

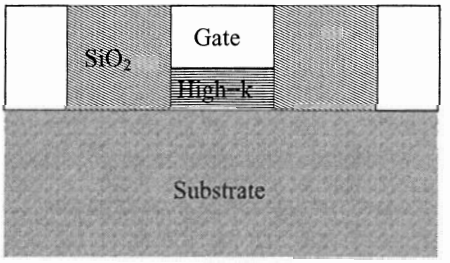

Fig. 3: Structure III

2.3 Static Analysis

At first, static analyses were carried out with Structure I, as this design shows the biggest deviation from the low-k device [4]. The different geometry of the high-k structure has a significant impact on the transfer characteristics of the device, which can be seen in Fig. 4. The increase of parasitic capacities leads to a reduction of the channel control. Depending on the k value of the high-k dielectric two effects can be observed, which will be analyzed in the following: A reduction of the slope of the transfer characteristics and a decrease of the threshold voltage.

An increase of the k-value increases the drain to channel capacitance, which adds an additional charge to the channel independently from the applied gate voltage. The additional charge causes a shift of the transfer characteristics to the left. This effect can be compensated by other measures like workfunction engineering in the gate or modification of the channel profile. So materials with an 'only-shifting' k value can be considered as alternative gate oxides.

The decrease of the slope can be interpreted as a general loss of channel control by the gate as the fringing fields and consequently the gate to drain/source capacitance increase. This effect can only be compensated by a variation of the stack geometry.

Fig. 5 shows the slope as function of k values for the IRTS device. The slope was extracted at an operating point with $V_{Gate} = 1.0V$. The degradation limit lies in the range of $k = 50$.

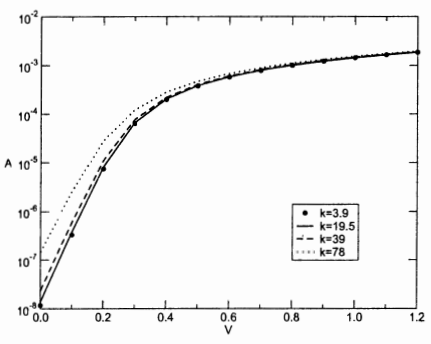

Fig. 4: Transfer Characteristics

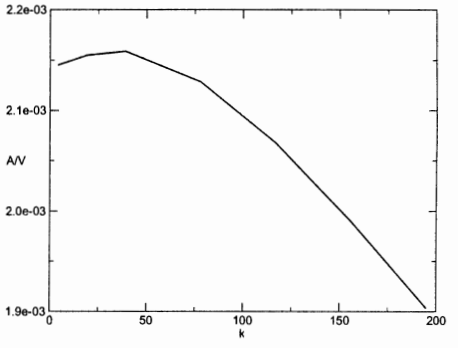

Fig. 5: Slope as Function of k-Value

2.4 Transient Analysis

The question of interest is, if the analysis of the transfer characteristics is significant for the transient device performance or not. The k-value used for the following simulation is 19.5. The deviance of the transfer characteristics is negligible in this case.

The delay time is closely linked to the contact capacities of the device, consequently an influence of the geometry on the obtained result is expected. The results show that the gate geometry has a significant impact on the delay time (Fig. 6), which increases by about 30% for Structure I. This result is remarkable as it cannot be expected from the static transfer characteristics, which showed almost no deviation between the results for

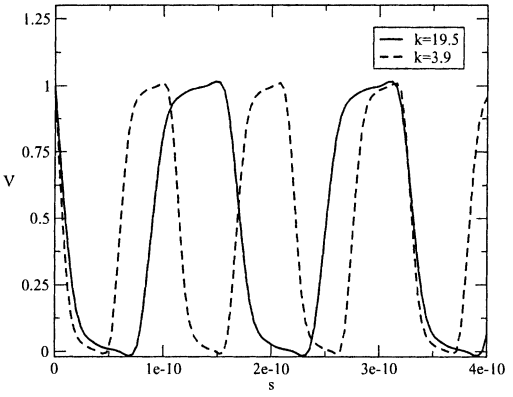

Fig. 6: Node Voltage for Different k-Values

the two devices (Fig. 4). It can be explained by an increase of the capacities between the gate contact and the drain/source doping due to the higher k-value of the gate oxide.

Due to the high computational time, the analyses for the other two structures were stopped at the first time step, but still the slope of the node voltage curve gives a clear indication of the device performance. The results of the replaced gate structure are identical to the simulations of the SiO_2 device ($\Delta V/\Delta t = 70.78\mathrm{V}/\mu\mathrm{s}$), but the planar structure already shows a clear decrease of the performance ($\Delta V/\Delta t = 67.82\mathrm{V}/\mu\mathrm{s}$), which is still comparatively high to the slope obtained for Structure I ($\Delta V/\Delta t = 51.28\mathrm{V}/\mu\mathrm{s}$), thus making Structure II and Structure III interesting candidates for the actual design of advanced CMOS devices.

3 Conclusion

It was shown that transient analyses offer a deeper insight into advanced CMOS devices compared to the static extraction of transfer characteristics. First analyses have been performed and it is expected that this method can serve as a powerful support for the development of future device generations.

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