Robust Method for Fast and Accurate Simulation of Random Dopant Fluctuation-Induced Vth Variation in MOSFETs with Arbitrary Complex Doping Distribution

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Abstract

We present a robust, fast, and accurate method for prediction of threshold voltage fluctuations induced by random placement of dopants in the MOSFETs. It is used to accurately predict the threshold voltage fluctuation for an analog transistor design. The method allows easy coupling to a process and device simulation framework, and, hence, evaluation of dopant induced threshold voltage fluctuation at the transistor design stage. The methodology is also used to compare the threshold voltage fluctuation in ultra-short channel devices having different profile architectures.

1 Introduction

Random dopant fluctuation-induced variation of threshold voltage in MOSFETs is a dominant source of mismatch in closely laid out analog transistors for current technologies. It is also one of major sources of parametric fluctuation in high-performance short-channel transistors and DRAM cell transistors, which have aggressively scaled gate areas and high doping concentration in channel. It is necessary for device designers to be able to predict the impact of changes in transistor design on sensitivity of the device characteristics to random dopant fluctuation. Accurate estimate of variance of device parameters induced by statistical doping fluctuations must also be obtained early in development cycle so that design manufacturability can be assessed.

2 New Method

Previous work in this area did not allow for fast and accurate prediction of dopant-induced variability in device structures with arbitrary complex doping distributions and meshes. Process development in most technologies takes place with the aid of TCAD where calibrated process and device simulators are coupled to evaluate impact of process changes on transistor performance. Process simulation of short channel devices in any technology result in devices where channel length (Leff) is much shorter than gate length (Lgate), and where complex doping profiles exist due

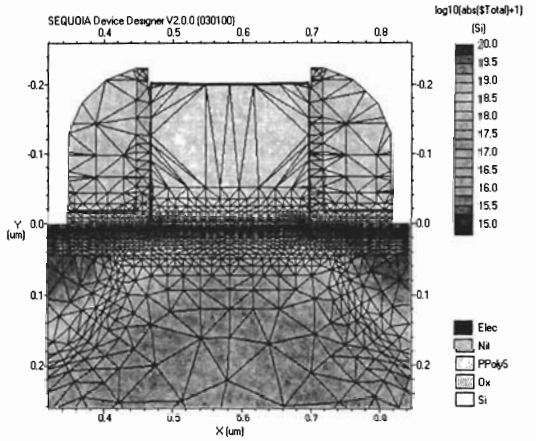

Fig.1. Device structure of a 0.25um gate length logic device showing rapidly varying doping profiles and a non-orthogonal simulation mesh.

to pocket implants and dopant diffusion mediated by extension defects. Furthermore, simulation grid in a realistic device structure obtained from process simulation must typically be replaced by non-uniform general triangular grid optimized for device simulation so that the device simulation is fast, robust and free from mesh-induced noise [2]. A typical device simulation mesh is shown in Fig. 1. Analytical models [3] cannot be used to derive parameter variation in such structures. Other more accurate methods involving use of 3D device simulation [1] are too slow for practical applications. Our method addresses both accuracy and speed issues and can be used with arbitrary doping profiles. It derives dopant-induced fluctuation from arbitrarily complex doping distributions and can be used with any mesh suitable for device simulation. Our algorithm calculates statistical doping fluctuation for each grid node based on the doping concentration at the node using binomial statistics (Fig. 2). Node area is calculated in a manner consistent with that used for descretization of PDE's in device simulator, and device width is

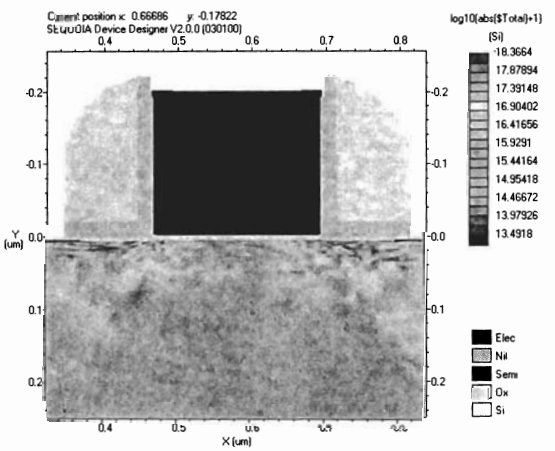

Fig.2. Random component of doping distribution obtained for structure in Fig.1 using method described here. This is superimposed on the nominal structure.

provided as user input. Nominal device structure is repeatedly subject to statistical perturbations followed by device simulation to extract important device parameters until sufficient statistical sample is obtained. Solution obtained from nominal device simulation is used as initial guess for perturbed device structures, allowing considerable speedup in extraction of device parameter variability.

3 Results

To demonstrate accuracy and efficiency of our method it was used to extract σ(Vt) for a 0.25um technology, using device profiles extracted using carefully calibrated process and device simulation. Excellent match between experimental and simulated data is observed (Fig.3). Quantum effects must be included to get proper match between experimental and simulated data. Note that the standard deviation of the Vt does not really scale at 1/Sqrt(Lgate), because Leff is typically much smaller than Lgate for shortest channel devices (see Fig. 4). The simulated variation with respect to width predicts a 1/sqrt(width) dependence.

As a practical application of this technique, impact of random dopant fluctuation on transistor characteristics for a 0.1um technology are used to compare robustness of several different device design options as shown in Fig. 5. Vertically graded profiles (retrograde) and laterally graded profiles (halo) are used to control short channel effects in ultra-short channel transistors. When compared at the same off-state leakage and threshold voltages, retrograde channel devices have lower dopant induced fluctuation, which is consistent with earlier predictions from analytical models [2]. Similar comparisons performed with realistic pocket profiles show that the dopant-induced fluctuation is a strong function of the pocket profile itself. If the pocket profile implanted at 30 or 45 degrees, and maintains it position as is common with heavier species like As or In, the induced fluctuations are smaller than with uniform profiles. However, if there is large dopant pileup at the surface, as is common with lighter pocket species like B, the induced fluctuations are much larger than in uniformly doped profiles. The results clearly indicate that there is much room for device designers to suitably tailor their device profiles to minimize such Vt fluctuations.

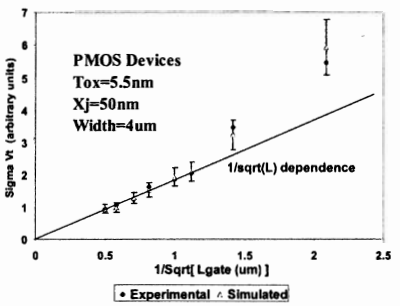

Fig.3. Experimental and simulated σ(Vt) versus length for device profiles descibed in Fig.1. Deviation from 1/sqrt(Lgate) trend at small channel

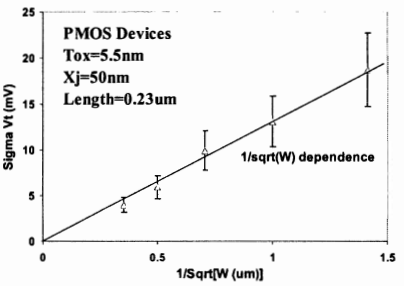

Fig.4. Binomially distributed fluctuation of dopants at each device node predicts dependence of σ(Vt) on width to be 1/sqrt(W)

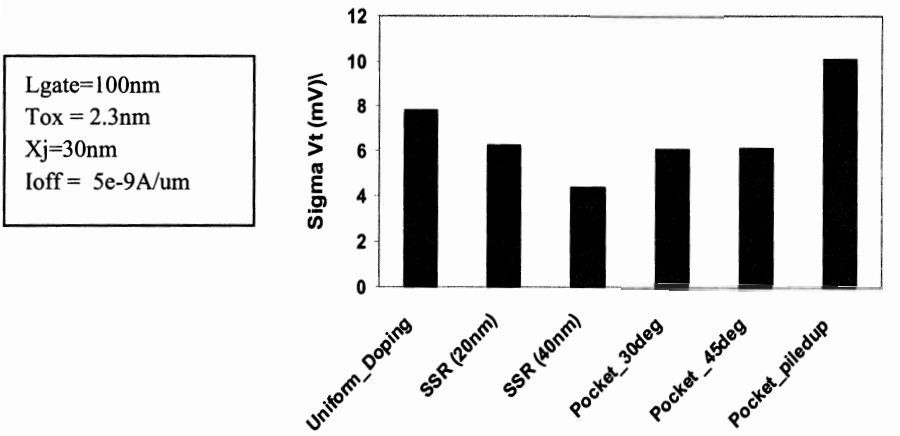

Fig.5. σ(vt) for realistic device profiles for a 100nm device, where doping levels have been adjusted in all profiles to have the same off-state leakage. Compared to uniform doping profile, retrograde channel with peak buried at 20nm has lower σ(vt). Increasing the peak depth to 40nm further reduces the Vt fluctuation. Profiles typical of angled pockets have lower σ(Vt) than uniformly doped devices. However, when the pocket dopant is allowed to couple with extension implant defects and diffuse, it piles up at the surface, and the resulting σ(Vt) is much higher.

4 Summary

A new method for fast and accurate simulation of the effect of statistical dopant fluctuations on MOSFET device characteristics has been developed. The method was used to simulate device performance variability of several different device architectures and proved to be both accurate and flexible.

References

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