# Decananometer FDSOI Device Optimization including Random Variation

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**Abstract**

Here, for the first time, is described a method for including random variability in device parameters for the benchmarking and optimizing of a decananometer fully-depleted silicon-on-insulator (FDSOI) device. The effect of interdevice and intradevice variability on device performance and design optimization is discussed. These methods are readily extendible to other devices and technologies.

## 1 Introduction

Despite the fact that stochastics are an issue of increasing importance at state-of-the-art device dimensions [1-5], they continue to be neglected in device benchmarking and in assessment of technology performance. In addition to the traditional variation in gate length, variation in other device dimensions and doping density are critical factors in determining circuit performance and therefore must be considered when optimizing a device design. The design yielding the best circuit performance may not be the one with the best typical-device behavior.

## 2 Stochastic Effects

Two principal device responses are leakage and drive. Static leakage current depends on both interdevice and intradevice variation, as it is integrated across width [3]. Whether, for a given leakage current density, there is a single device of width $N \times W$ or $N$ devices each of width $W$ is unimportant.

Circuit performance will depend more on device-to-device variation than on variation across an individual device. In [1], a value of two standard deviations below the mean drive current was used to predict the performance of a simple parallel set of delay chains. However, the appropriate standard deviation is the interdevice, not intradevice, value. For example, applying the standard deviation of gate length as extracted from single cross-sectional SEM's from different devices could lead to an overestimation of interdevice variability, as it includes intradevice variability, as well.[1]

## 3 Method

### 3.1 Evaluation

To account for stochastic variation, devices are simulated for different representative values of the device parameters. The accumulated results, appropriately weighted, are used to generate, for each $V_D$ and $V_G$, values of $\langle I_D \rangle$, $\langle \ln I_D \rangle$, and $\sigma_{\ln Id}$. The gate voltage yielding the target $\langle I_D \rangle$ is determined and a fixed $\Delta V_G = 1\,\mathrm{V}$ overdrive is applied, at which point the $V_D = V_{Dlin} = 0.1\,\mathrm{V}$ and $V_D = V_{DD} = 1.5\,\mathrm{V}$ values of $\exp\left[\langle \ln I_D \rangle - 2\sigma_{\ln id}\right]$ are interpolated. A weighted

[1] This assumes cross-section positions are uncorrelated with intradevice gate length variation.

harmonic mean is calculated as the final benchmark, weighting the $V_D = V_{DD}$ to $V_D = V_{Dlin}$ values in an 8:1 ratio[2].

### 3.2 Parameter Space Sampling

To economize on simulations, a principle axis sampling strategy was selected as a discrete approximation to a continuous normal distribution. In one dimension, samples taken at $\Delta x \in (0, \pm\sqrt{3}\sigma)$, with weights of $(1, 4, 1)$ for $\Delta x \in (-1, 0, 1)\sqrt{3}\sigma$, yield matching of normal values of $\langle \Delta x^n \rangle$ through $n = 5$. For more than one dimension, points are sampled at $\Delta x_i \in (\pm\sqrt{3}\sigma)$ for $i$ along each principle axis in turn, with $\Delta x_{j \neq i} = 0$, and at the center point. Samples are then given unity weight with the exception of the center point, which is weighted $6 - 2n$, where $n$ is the number of dimensions. This results in the correct values of $\langle \Delta x_i^n \rangle$ through $n = 5$, for all $i$. It may, however, neglect the effect of deviations from normal behavior for large deviates, such as a catastrophic failure at a $3\sigma$ subnominal dimension.

## 4 Examples

### 4.1 $L_G$, $t_{Si}$, $t_{box}$

Simulations were performed using Medici version 2000.2.1 by Avanti with the *shiramob* mobility model and the *fldmob* longitudinal field dependence. No explicit quantum mechanical effects were considered; these will be addressed in a future work.

For all simulations the source and drain are length 50 nm, doped $10^{20}/\mathrm{cm}^3$ $n$-type, and aligned to the gate edge.

Results are shown versus gate length, silicon thickness, and buried oxide thickness in Figure 1. In each case, plots are shown for the case where variation is neglected and for the case where the $x$-axis parameter is assumed to be random with the appropriate $\sigma$ and statistical dopant fluctuation, if the body is doped, is modeled. For $t_{box}$ and $t_{Si}$, it is assumed all variation is interdevice, while for $L_G$, it is assumed the variance is partitioned equally between interdevice and intradevice components. Variation in doping, where applicable, is analytically estimated as described later. Note in each case the inclusion of stochastic effects into the analysis has a substantial effect on dependence of the benchmark on the associated parameter.

### 4.2 Gate Oxide Thickness

The same device, with $n_{Si} = 0$, $L_G = 50$ nm, $t_{Si} = 10$ nm, $t_{box} = 20$ nm, and $t_{ox} = 2$ nm, had its interdevice oxide variation varied from 0 to 0.3 nm. Since gate oxide thickness has such a strong influence on device performance, the variance in response associated with a variance in gate oxide thickness, both in the subthreshold and superthreshold regions, is substantial. To good approximation, the metric was degraded 6.5% for each 0.1 nm increase in $\sigma_{tox}$.

### 4.3 Silicon Doping

For the purposes of this work an analytic approximation to the effect of stochastic variation of atomic dopants on the effective doping density in

[2] This is intended to be a typical ratio; the optimal ratio is dependent on the circuit and on $V_{DD}$ and $V_{Dlin}$.

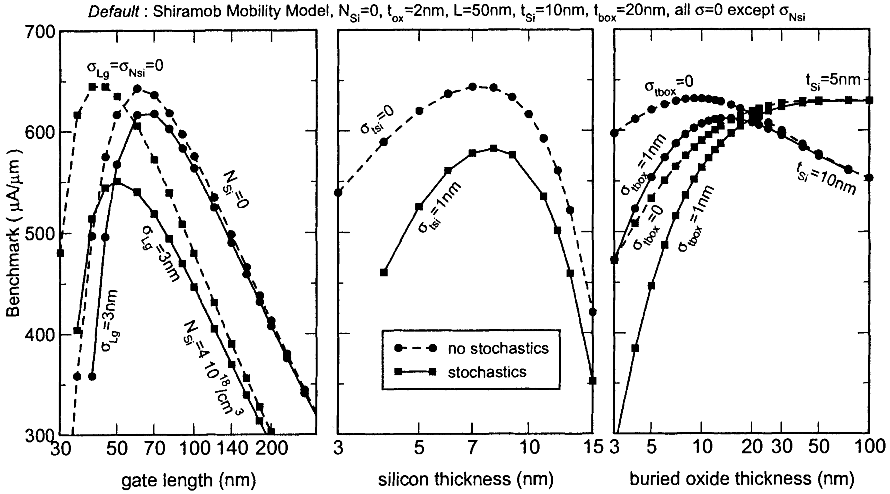


**Fig. 1.** Comparison of benchmark versus various parameters with and without modeling of variation of the $x$-axis parameter. In $L_G$ plot, when gate length variation is suppressed, so is dopant stochastic modeling.

a slice of the channel, based on simple electrostatic analysis, was used[3], $\sigma_N^2 = N/\left[L_G t_{Si}\left(t_{Si} + 4t_{ox}\right)\right]$. Carriers traversing the channel along an interface segment from source to drain are considered to see an effective doping level proportional to the number of dopant atoms in a trapezoidal solid, roughly the set of channel points electrostatically closer to the segment than to the gate electrode, assuming $\epsilon_{Si}/\epsilon_{ox} = 3$. Thus the doping level is subject to local fluctuations in proportion to the Poisson-statistical variation in the atom count within the trapezoidal solid. The interdevice component of the resulting variance in the device response is in proportion to the ratio of the volume of this trapezoidal solid to that of the device body.

Figure 2 shows results of devices with either no stochastic analysis or stochastics applied only to doping. Note while higher doping is observed to help the performance of thicker-silicon devices when stochastics are neglected, the short-channel-effect benefits of the doping are offset when the modeled doping stochastic effects are included. Curves are shown both with and without mobility modeling to isolate the electrostatic/stochastic tradeoff.

## 4.4 Multivariate Optimization

Optimization of $L_G$, $t_{Si}$, $t_{box}$ simultaneously, with $\sigma_L = 3\,\text{nm}$ (50% interdevice variance), $\sigma_{tox} = \sigma_{tsi} = 1\,\text{nm}$ (100% interdevice variance), and $n_{Si} = 0$, yielded an optimal design of $L_G = 70.56\,\text{nm}$, $t_{Si} = 10.35\,\text{nm}$, and $t_{box} = 27.64\,\text{nm}$, with a benchmark current $I_{Dtest} = 600.4\,\text{nA}/\mu\text{m}$. When doping was allowed to vary as well, the optimal design had[4] $n_{Si} = 1.1 \times 10^{18}/\text{cm}^3$, $L_G = 69.5\,\text{nm}$, $t_{Si} =$

[3]This is intended to have the correct qualitative behavior. For better quantitative accuracy, validation against 3-d Monte Carlo simulations should be done. The formula assumes zero source/drain-to-gate overlap, consistent with the abrupt junctions used in this study.

[4]Reduced precision is provided due to the additional degree of freedom in the parameter space.

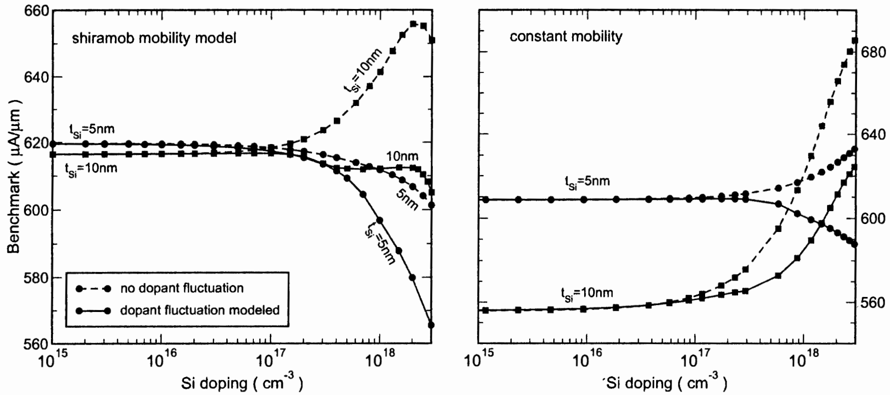


**Fig. 2.** Comparison of benchmark versus doping with and without modeling of statistical dopant fluctuations for $L_G = 50\,\mathrm{nm}$ FDSOI nFETs with $t_{Si} = 5\,\mathrm{nm}$ or $10\,\mathrm{nm}$, $t_{box} = 20\,\mathrm{nm}$. Plots are shown for *shiramob* mobility model and for a fixed electron mobilitie of $100\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{sec}$. The latter doesn't include the the effect of ionized impurity scattering with increaing doping density.

16.5 nm, and $t_{box} = 17.9\,\mathrm{nm}$, yielding $I_{Dtest} = 603\,\mathrm{nA}/\mu\mathrm{m}$. A small performance improvement was gained by exploiting the improved short channel immunity of doped films, which allowed the silicon thickness to be increased, decreasing series resistance. At higher doping levels, the effect of doping stochastics and ionized impurity scattering cause a significant reduction in the benchmark from the optimal value.

## 5 Conclusion

Proper benchmarking is critical to device design optimization. The determination of a figure of merit to be optimized must include consideration of the variation of as well as the nominal value of device parameters. Variation includes both interdevice and intradevice components, each of which affect performance differently. Fully depleted silicon on insulator devices were examined, focusing on the effects on performance of gate length, buried oxide thickness, silicon thickness, and body doping. In each case modeling of the effects of variation in the parameters had a substantial influence both on the optimal choice of the parameter and on the performance expected at the optimal parameter value. Control of gate oxide thickness was also seen to be critical to performance.

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## References

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