3D Statistical Simulation of Intrinsic Fluctuations in Decanano MOSFETs Introduced by Discrete Dopants, Oxide Thickness Fluctuations and LER

Asen Asenov
Department of Electronics and Electrical Engineering, University of Glasgow
Glasgow G12 8LT, Scotland, UK
A.Asenov@elec.gla.ac.uk

Abstract

The need for statistical 3D simulations to study intrinsic parameter fluctuations in aggressively scaled MOSFETs introduced by discreteness of charge and atomicity of matter is discussed. We describe a hierarchical implementation of such a 3D 'atomistic' simulation approach, which includes quantum mechanical corrections based on the Density Gradient algorithm. Simulation examples of intrinsic parameter fluctuations associated with random discrete dopants in the active region of the device and in the polysilicon gate, oxide thickness fluctuation within the gate area, and line edge roughness (LER) of the gate are presented. We speculate about the challenges ahead in understanding and accurately simulating the atomistic effects in the next generation of MOSFETs.

1 Introduction

The International Technology Roadmap for Semiconductors [1] forecasts that semiconductor devices will reach decanano (i.e. sub-100 nm) dimensions in the first decade of the new millennium. At the same time, doubts have been expressed by leading IC manufacturers, such as Intel [2], that conventional device architectures can be scaled to deep decanano dimensions and that Moore's Law can be maintained. It becomes extremely important to examine, by means of predictive device modelling and simulation, possible scaling scenarios, pitfalls, and promising device architectures in order to give direction to the urgently needed, and very costly, technology developments of the next decade, and thus save unnecessary effort and expense. Predictive modelling and simulation face numerous challenges associated with the complex geometry, high fields, non-equilibrium transport and quantum effects exhibited by any decanano device architecture.

A fact not yet widely realised is that the scaling of devices in integrated circuits will reach a stage where the granularity of the electric charge and the atomicity of matter begin to introduce substantial 'intrinsic' variation in individual device characteristics, and must be included in the simulations. The variation in number and position of dopant atoms in the active region of MOSFETs will make each transistor microscopically different and introduce significant intrinsic parameter variation from device to device on a single chip [3]. In addition, the gate oxide thickness becomes

equivalent to several atomic layers with a typical interface roughness of the order of 1-2 atomic layers [4]. This will introduce a substantial variation in the oxide thickness in the gate region resulting in a microscopically different oxide thickness pattern in each transistor. The unique pattern of the oxide roughness in each decanano MOSFET will affect both device electrostatics and the surface roughness limited mobility from device to device. The granularity of the gate material and the photo-resist, together with other factors, will introduce unavoidable roughness in the gate pattern definition and statistical variations in geometry between devices. When combined together the variations in dopant statistics, oxide thickness pattern, gate material and geometry will have a crucial impact on the functionality, yield and reliability of the corresponding circuits and systems.

From discreteness of charge to granularity of material, in this paper we survey some of the significant aspects of the atomistic picture of MOSFETs in the sub-100 nm regime. We will first highlight important, and practical, issues pertaining to the 3D atomistic simulator development in a statistical and quantum mechanical framework. This will be followed by a series of simulation results highlighting the effects of discrete dopants, rough interfaces and imperfect definition of edges on the intrinsic parameter fluctuations in decanano MOSFETs. Finally, we will point out issues with regard to 'atomicity' and simulator development in MOSFETs that require further attention.

2 Simulation approach

The statistical, atomic scale variations in decanano devices shifts the paradigm of numerical device simulations [5]. It is no longer sufficient to simulate a single device with continuous doping distribution, uniform oxide thickness and unified dimensions to represent one macroscopic design. Each MOSFET is microscopically different at the level of dopant distribution, oxide thickness and gate pattern, so an ensemble of macroscopically identical but microscopically different devices must be characterised. The aim of the numerical simulation shifts from predicting the characteristics of a single device towards estimating the mean values and the variance of basic device parameters, such as threshold voltage, subthreshold slope, transconductance, drive current, etc. for a whole ensemble of microscopically different devices in the system. It must be emphasised that even the mean values obtained from statistical atomistic simulations are not identical to the values corresponding to continuous charge simulation [6, 7]. The simulation of a single device with random dopants, oxide thickness and gate pattern variation requires a 3D solution with fine grain discretisation. The requirement for statistical simulations transforms the problem effectively into a four dimensional one where the fourth dimension is the size of the statistical sample.

We use drift diffusion (DD) simulations to study intrinsic parameters fluctuations in decanano MOSFETS. Quantum mechanical confinement effects in the inversion layer are taken into account using the density gradient (DG) formalism [8, 9]. The drift-diffusion approach does not properly represent the non-equilibrium carrier

dynamics and ballistic transport effects and hence underestimates the drain current. However, it can be used with confidence to estimate the threshold voltage based on a current criterion in the subthreshold region, where the current is exponentially controlled by the gate and its underestimation produces a minute error in the calculated value for the threshold voltage. Above threshold the quantum corrected DD simulations provide a sufficiently accurate estimate for the variation in the device parameters resulting from the electrostatics of random discrete dopants, local oxide thickness variations and LER.

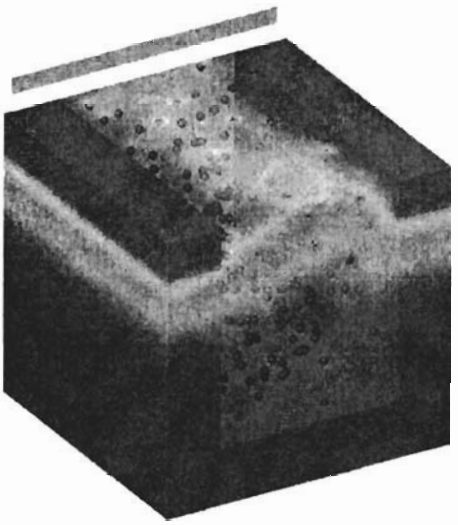

Fig. 1. Potential distribution at threshold voltage obtained from atomistic DG simulations of a 30×50 nm MOSFET.

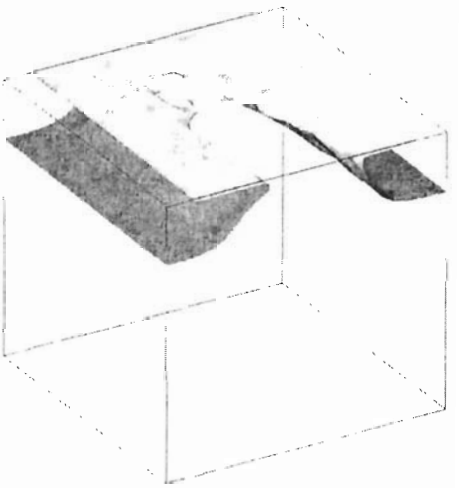

Fig. 2. One equi-concentration contour corresponding to the potential distribution in Fig. 1.

A typical atomistic solution domain is shown in Fig 1. The discrete dopants are placed in the outlined channel region between the source and drain. In the rest of the simulation domain the doping charge has a continuous distribution. Although the best way to introduce the doping distributions in the atomistic simulations would be to use the output from an atomic scale process simulator [10], we use a simpler approach. The expected number of dopants in the atomistic region is estimated by integrating the continuous doping distribution, obtained for example from a standard process simulator. The actual number of dopants in each MOSFET from the simulated ensemble is chosen randomly from a Poisson distribution with the above mean. Then, using a rejection technique, the dopants are placed randomly according to the initial continuous doping distribution. The potential distribution at gate voltage equal to the threshold voltage is superimposed in Fig. 1. Strong potential fluctuations at the Si/SiO_2 interface associated with the discrete dopants can be observed. The current in the device percolates through the valleys of the potential landscape. One electron equi-concentration contour which corresponds to this solution is presented in Fig. 2. The equi-concentration contour highlights the basic features of the quantum charge distribution. The quantum confinement in the channel

results in a smoothing of the carrier density profile with a maximum in the electron concentration, located approximately 1.5 nm below the interface.

3 Random discrete dopants

The dependence of the threshold voltage on oxide thickness, obtained from classical and quantum DG simulations, is presented in Fig. 3 for a 50×50 nm MOSFET. With channel doping concentration 5×10^{18} cm^{-3}. Such devices have an average of 170 atoms in the channel depletion region. Samples of 200 microscopically different devices are simulate to extract the average threshold voltage and its standard deviation for each macroscopic combination of device design parameters. Results for the average threshold voltage, obtained from atomistic simulations, and for the threshold voltage, obtained from continuous charge simulations are compared for metal and poly-silicon gate devices. The quantum mechanical threshold voltage shift decreases with the reduction in the oxide thickness t_{ox}. The inclusion of the poly-Si gate in the simulations results in an additional increase in the threshold voltage. Most importantly the random dopant induced threshold voltage lowering, inherent to the atomistic simulations, and associated with percolation of the channel current through valleys in the potential fluctuations, increases in the quantum case.

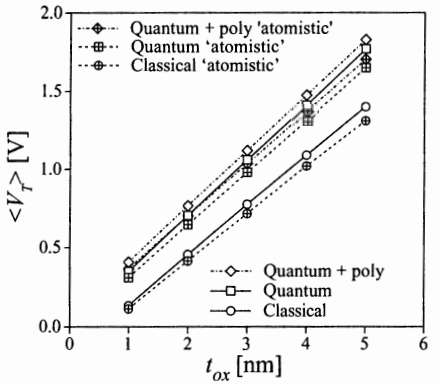

Fig. 3. Dependence of average threshold voltage on the gate oxide thickness in a 50×50 nm MOSFET.

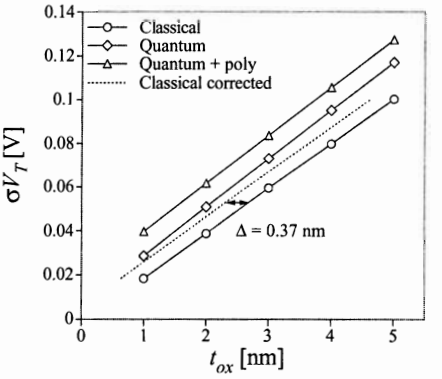

Fig. 4. Threshold voltage standard deviation as a function of the oxide thickness in a 50×50 nm MOSFET.

The dependencies of the threshold voltage standard deviation, σV_T, as a function of the oxide thickness, extracted from classical and from quantum atomistic simulations, are compared in Fig. 4. In the classical simulations of metal gate devices σV_T scales linearly to zero with the corresponding scaling of t_{ox} as a result of the screening from the gate. The values of σV_T corresponding to the quantum simulations are shifted up with respect to the classical simulations, and the shift increases slightly with the increase in the oxide thickness. The inclusion of the poly-silicon gate in the simulations results in an additional increase in σV_T, which, in combination with the increase associated with the quantum mechanical effects,

almost doubles the fluctuations for oxide thicknesses below 2 nm. Thus the inclusion of quantum effects paints a more pessimistic picture than anticipated until now from purely DD simulations.

4 Oxide thickness fluctuations

In decanano MOSFETs the gate oxide thickness will be equivalent to a few silicon atomic layers with a typical interface roughness of one to two atomic layers [11]. The roughness can introduce more than 50% variation in the oxide thickness in devices with a 1 nm gate oxide. The unique random pattern of the gate oxide in each MOSFET, and the related surface landscape and potential fluctuations, will have a substantial contribution to the intrinsic parameter variation in such devices. A typical random Si/SiO_2 interface used in the simulation of a 30×30 nm MOSFET, is shown at the top of Fig. 5. The interface has been re-constructed using a 2D Fourier synthesis approach and a power spectrum corresponding to a Gaussian correlation function. Continuous charge was used, and only roughness of the Si/SiO_2 interface was introduced in the simulations. The potential distribution at threshold voltage is shown at the bottom of the same figure. One equiconcentration surface corresponding to electron charge density 1×10^{17} cm^{-3} is plotted in the middle illustrating the quantum confinement effects in both vertical and lateral directions.

The dependence of the threshold voltage standard deviation σV_T on the correlation length Λ obtained from classical and DG simulations is compared in Fig. 6. The

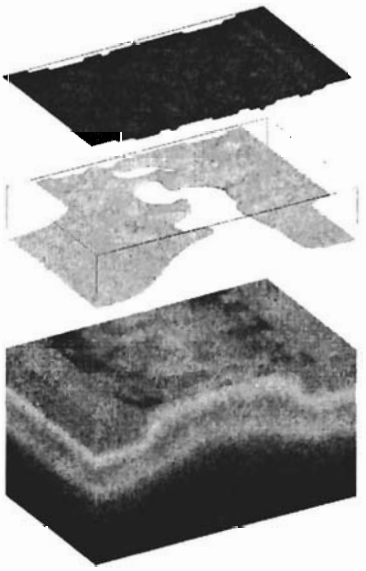

Fig. 5. The profile of the random Si/SiO_2 interface in a 30×30 nm MOSFET with t_{ox}= 1 nm (top), an equiconcentration contour obtained from DG simulation and the potential distribution (bottom).

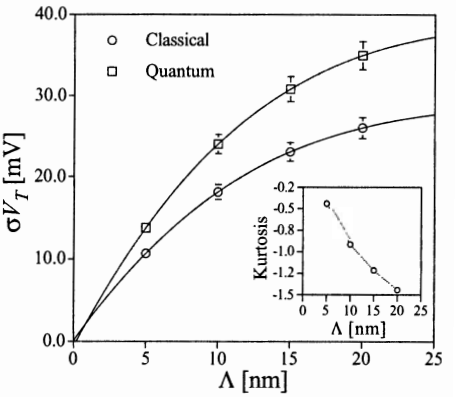

Fig. 6. Dependence of the threshold voltage standard deviation σV_T on the correlation length Λ for the 30×30 nm MOSFETs as in Fig. 5. Classical and DG simulation results are compared.

introduction of quantum corrections results in an increase in the threshold voltage variation. We believe that this is related to the lateral confinement effects, which narrow the current percolation paths. In both cases the dependence of σV_T on Λ is linear for correlation lengths much smaller than the characteristic MOSFET dimensions and saturates for large Λ. The dependence of the kurtosis of the threshold voltage distribution as a function of Λ in the DG case is presented as an inset in the same figure. The increasingly negative values of the kurtosis are an indication for the flattening of the σV_T distribution with the increase in correlation length. For devices with characteristic dimension below 30 nm the oxide thickness induced threshold voltage fluctuations become comparable to the fluctuations induced by random discrete dopants, particularly when the contribution of the both interfaces is taken into account and the larger correlation length suggested by AFM measurements are adopted.

5 Line edge roughness

Line edge roughness (LER), resulting from granularity of resists and gate material and from factors limiting the tool performance used in lithography processes, is difficult to reduce below 5 nm. As the aggressive scaling of Si MOSFETs continues to the sub-100 nm regime LER will constitute a large fraction of the gate length and will introduce significant intrinsic variations in the device parameters in its own right. As a natural extension to the statistical 3D simulations described in this paper, we approach the simulation of LER in decanano MOSFETs in a statistical fashion. LER in the simulations is specified by rms amplitude, Δ, and correlation length, Λ. This allows both 3D and statistical aspects of LER to be naturally incorporated in a single simulation framework. The reconstruction of realistic gate edges is based on a 1D Fourier synthesis approach, similar to that used in the generation of the Si/SiO_2 interface. A typical 30×30 nm MOSFET with continuous doping and LER is shown in Fig.7 for Λ = 10 nm and LER = 3Δ = 6 nm.

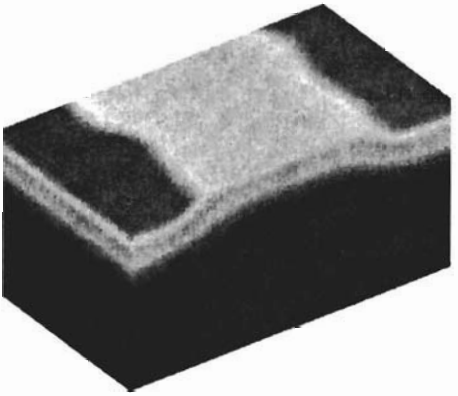

Fig. 7. Potential distribution at threshold in a well scaled 30×30 nm MOSFET with line edge roughness of the gate of 6 nm.

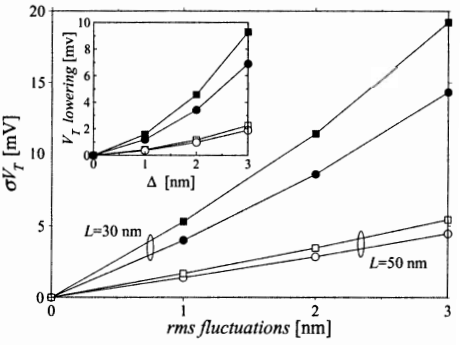

Fig. 8. Threshold voltage fluctuations associated with LER as a function of the rms amplitude Δ.

LER causes threshold fluctuations similar to those resulting from random dopants or oxide thickness fluctuation, as can be seen in Fig. 8. Fluctuations increase when Λ or Δ is increased. The average threshold voltage is also affected, with a pronounced threshold voltage lowering taking place. The fluctuations are comparable in magnitude to those resulting from random dopants in similar devices.

6 The challenges ahead

In any simulation, the accuracy is only as good as the description of the simulation domain and the complexity of various physical models in use. Hence, predictive atomistic process simulators should be natural companions to further attempts in atomistic device modelling, providing atomic scale information for the device structures. A main challenge in studying decanano devices therefore lies in interfacing the atomistic device modelling tools with predictive atomistic process simulations, resulting in a more reliable description of the problem at hand.

Based on the same philosophy, improvements to the physical models employed in the transport problem are also required. For instance higher-moments of the Boltzmann transport equation such as hydrodynamic models may be incorporated in the atomistic simulations to correctly account for the non-equilibrium conditions in decanano devices. Particle simulations may be especially useful to uncover effects related to the discrete nature of carriers and noise, which would affect the device performance at an atomistic level, and to resolve *ab-initio* long range electrostatic effects, carrier-carrier and carrier-impurity interactions. More elaborate or exact treatment of quantum effects is still missing in our simulations. At present, the trade off is between the efficiency of numerical simulations and the range of applicability in quantum mechanical simulation strategies.

The increased understanding of different components of fluctuations in device characteristics points to an increasing need for developing new device architectures that can suppress them. Several novel device concepts such as double gate MOSFETs or SiGe heterojunction MOSFETs must be simulated to assess their immunity to atomistic processes. Ultimately, the device performance is affected by the interplay of many different sources of fluctuations discussed within this paper. Thus, the correlation between the contributions of different components of fluctuations should be investigated in atomistic simulations by concurrently incorporating different processes in a single device. In doing so, any other processes which are relevant to the decanano regime, but have not been treated fully here, must also be included.

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