Bipolar Transistor's Intrinsic and Extrinsic Capacitance Determination

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Abstract

We present a new method to determine the intrinsic and extrinsic base-emitter and base-collector junction capacitances parameters of bipolar transistors as a function of junction bias. The capacitance specific compact model parameters (C_{j0}, V_j,γ_j) can be extracted for the intrinsic as well as for extrinsic part. The results can be introduced in recent compact bipolar models.

1 Introduction

Parasitics in bipolar transistors are becoming of great importance due to the reduction in the device dimensions. Therefore, the junction capacitances distributed nature has to be studied, because it affects the device HF behaviour, but also the DC behaviour via the direct and inverse Early effect. The recent bipolar compact models (Hicum [1], Mextram [2], VBIC [3]) take this effect into account by using a distributed R-C network (junction capacitance splitting across the base resistance). All compact models describe the junction capacitance behaviour under reverse and low forward bias with the relation:

$$Cj = C_{j0} \Big/ \left(1 - \frac{V}{Vj}\right)^{\gamma j} \qquad (1)$$

The capacitance splitting implies the need of two different equations (1) and the corresponding junction parameter sets (C_{j0}, V_j, γ_j) for the intrinsic and extrinsic capacitances. To determine the intrinsic and extrinsic part of the junction capacitances, several methods exist:

1) The first one consists in evaluating the capacitances parameters using a device simulator. Nevertheless, a direct method would be preferred since parameter extraction in real world compact modelling is always based on electrical measurements.

2) The second method is described in [2]. It allows an approximated partitioning of the zero bias capacitance only for the BC junction, considering that the intrinsic and extrinsic junctions have the same characteristics, and consequently the same junction parameters, which is not true, especially in the case of SIC implant. Additionally, this method is particularly sensitive to previous parameter extraction errors.

3) The third method is described in [3]. It consists in a geometrical analysis of the junction capacitances: The intrinsic and extrinsic capacitances are considered to be proportional to an effective junction area and an effective perimeter, respectively. Therefore, the effective geometry

has to be known precisely, which is not always possible. Moreover, for the B-C junction, especially if a SIC implant exists, this method looses its physical meaning and is no more valid. Therefore, in the following section, we present a new self consistent method, based on HF measurements, that allows to split the capacitances values into an intrinsic and an extrinsic part.

2 Direct Extraction Procedure

Under reverse and low forward bias conditions for all junctions, the following assumptions can be made:

(a) the transistor is supposed to have no transfer current, which implies infinite values for $r\pi$ and $r\mu$, and that the diffusion capacitances C_{de} and C_{dc} can be neglected, giving the equivalent circuit of figure 1.

(b) since the transistor has no current gain, the influence of the series resistance re, and rc are further neglected, and rbx is lumped with rb. The resulting simplifications give the Y-parameters of interest:

$$\mathrm{Re}(Y_{11}) = \frac{1}{rb}\frac{\left(\frac{\omega^2}{1/rb\,(Cjei+Cjci)}\right)^2}{1+\left(\frac{\omega}{1/rb\,(Cjei+Cjci)}\right)^2} \qquad \mathrm{Re}(Y_{11}+Y_{12}) = C_{jei}\frac{\left(\frac{\omega^2}{1/rb\,(Cjei+Cjci)}\right)}{1+\left(\frac{\omega}{1/rb\,(Cjei+Cjci)}\right)^2} \quad (2)$$

The first step of the method is a classical junction capacitance determination using S-parameters. The total junction capacitances $C_{jeT}(V_{be})$ and $C_{jcT}(V_{bc})$ are determined using well known relations:

$$C_{jcT} = \frac{\mathrm{Im}(-Y_{12})}{\omega} \qquad C_{jeT} = \frac{\mathrm{Im}(Y_{11}+Y_{12})}{\omega} \quad (3)$$

with $C_{jeT} = C_{jei} + C_{jex}$ and $C_{jcT} = C_{jci} + C_{jcx}$. We can note that the result depends greatly on the frequency used for measurements, as show figure 2 where $C_{jcT}(f)$ and $C_{jeT}(f)$ are plotted.

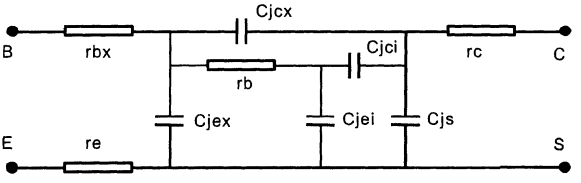

Figure 1: equivalent circuit for "Y-parameter determination"

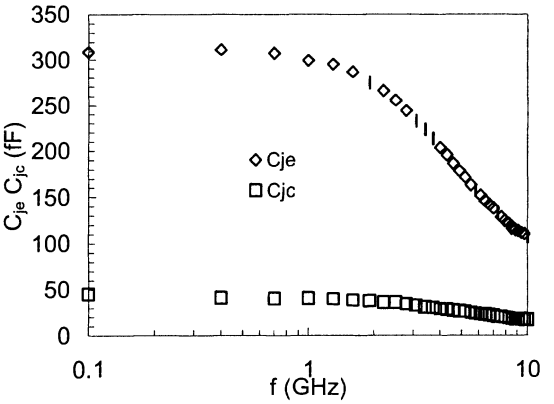

Figure 2: $C_{jcT}(f)$ and $C_{jeT}(f)$ equation 3

The second step of the method is based on the same measurements, using a higher frequency range. Moreover, (2) can be rearranged as:

$$\frac{\omega^2}{\mathrm{Re}(Y_{11})} = rb\,\omega_T^2 + rb\,\omega_T\,\omega^2 \qquad \frac{\omega^2}{\mathrm{Re}(Y_{11}+Y_{12})} = \frac{\omega_T}{Cjei} + \frac{\omega^2}{\omega_T\,Cjei} \qquad (4)$$

$$\text{with } \omega_T = 1/\,r_b\left(C_{jei}+C_{jci}\right)$$

Plotting $\omega^2/\mathrm{Re}(Y_{11})$ and $\omega^2/\mathrm{Re}(Y_{11}+Y_{12})$ versus $\omega^2=(2\pi f)^2$ and applying a linear regression allows to determine rb, Cjei and Cjci. As an example, figure 3 (a) shows the plots of $\omega^2/\mathrm{Re}(Y_{11})$ and $\omega^2/\mathrm{Re}(Y_{11}+Y_{12})$ versus ω^2 for V_{bc}=0 and V_{be}=0. We can note that the curves are nearly straight lines, which confirms the validity of the equivalent circuit used to derive (2) and (4).
The determination of Cjei and Cjci can be performed for each bias point, then allowing the determination of Cjei and Cjci voltage variation and the related junction parameters extraction (C_{j0}, V_j,γ_j) by using a standard method.
The extrinsic capacitances are determined using: $C_{jex}=C_{jeT}-C_{jei}$ and $C_{jcx}=C_{jcT}-C_{jci}$.

3 Results

The method was applied to advanced SiGe heterojunction bipolar transistors fabricated by ST Microelectronics, having a 45 GHz transit frequency and a current gain of 150. The transistors are realised in a self aligned technology with SIC implant and 0.4µm minimum emitter width.
Figure 3 (b), shows the extracted C_{jei}, C_{jex}, C_{jci} and C_{jcx} versus junction voltage for a 1.6x25.6 µm² emitter bipolar transistor. The extracted base resistance rb=105 Ω at zero bias. Moreover, the comparison of the results for transistors of different sizes have shown the scaling coherence of this approach.

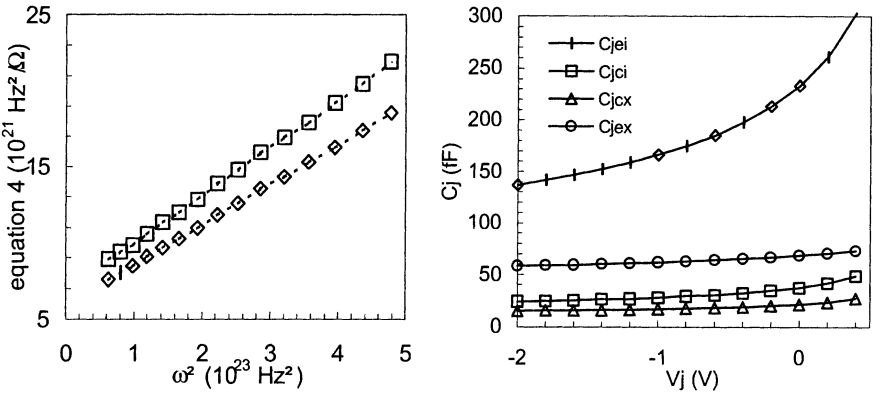

Figure 3: (a) $\omega^2/Re(Y_{11})$ and $\omega^2/Re(Y_{11})$ vs ω^2 **(b)** C_{jei} and C_{jci} versus V_{be} and V_{bc}

4 Conclusion

A new method for bipolar transistor's intrinsic and extrinsic capacitances parameter determination is presented. These parameters are essential for recent bipolar compact models. This splitting is an important improvement for the high frequency behaviour modelling and for the output conductance modelling (in the Hicum and Mextram model the Early effect depends on the intrinsic capacitances). This method has the advantage to be a direct method, based on measurements, which is physically more accurate for a given device than methods based on test structures and geometry considerations. Furthermore, a full electrical device modelling has been performed using the Hicum model, and we got excellent results for both, DC and AC characteristics.

References

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