Modelling of High-Voltage SOI-LDMOS Transistors including Self-Heating

A.C.T. Aarts, M.J. Swanenberg* and W.J. Kloosterman*

Philips Research Laboratories, Eindhoven, The Netherlands
* Philips Semiconductors, Nijmegen, The Netherlands

Abstract
This paper presents (i) the compact modelling and (ii) the parameter extraction strategy of a 12 V SOI-LDMOS transistor. The LDMOS transistor is characterized by a macro model consisting of the physics based Philips' MOS Model 9 (MM9) for the channel and MOS Model 31 (MM31) for the drift region. Incorporation of the effect of self-heating during parameter extraction shows that the DC-characteristics can be described consistently and accurately over a wide range of biases, temperatures and device dimensions.

1 Introduction

The use of SOI (Silicon-On-Insulator) in a high-voltage process provides a new technology for consumer and automotive applications [4]. The advantage of SOI comprises, amongst others, latchup-free operation, a high packing density and less leakage current at high temperature operation. Optimal design of these high-voltage IC-applications requires accurate models for circuit simulation, describing the characteristics of the high-voltage devices over a wide range of biases, temperatures and device dimensions. Due to the combination of SOI and high-power densities, the self-heating of the device is significant. Therefore, a model that accounts for the temperature rise due to self-heating is essential for reliable results. In contrast to [2] where the effect of self-heating has been limited to the drift region, we incorporate self-heating in the drift region as well as in the channel. In addition to [1] where self-heating has also been included in an SOI-LDMOS model, this paper presents the parameter extraction strategy as well as the full scalability of an SOI-LDMOS model over a range of temperatures and device dimensions.

2 SOI-LDMOS Technology

Fig. 1 shows the cross-section of a 12 V n-channel LDMOS transistor in SOI (gate-oxide thickness is 38 nm). The p-well is diffused under the gate to about 1 μm from the source. The drift region of lightly doped n-type Si is necessary to sustain the high voltages. For characterization purposes the p-well body contact is separated from the source contact. The transistor is isolated by LOCOS as well as by a thick buried oxide (box) layer (of thickness t_{box} = 1 μm) underneath the SOI-layer. The length L_{box} of the SOI-layer is approximately 27 μm.

In forward operation electrons from the inversion channel in the p-well body are transported through the drift region to the drain contact. The formation of an accumulation layer under the gate in the drift region decreases the resistance, whereas the depletion layer at the p-well/drift region junction increases this resistance. For higher drain voltages the current is also decreased by depletion at the surface of the drift region from the drain side.

3 LDMOS Modelling

Fig. 2 shows the macro model used for DC-characterization of the 12 V SOI-LDMOS transistor. The channel in the p-well is modelled by MM9, whereas the n^- drift region is modelled by MM31 [3]. The latter is a depletion and accumulation mode MOSFET model, including velocity saturation, pinch-off and temperature effects. It describes the MOS-action of the gate field plate above the n^- drift region, as well as junction-depletion from the p-well body. In the macro model, the small influence of a bias at the Si-substrate is neglected. Notice that in most bias regimes this macro model can also be used for AC-characterization.

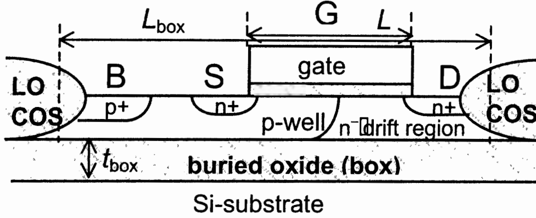

Fig. 1. Cross-section of the 12 V n-channel SOI-LDMOS transistor.

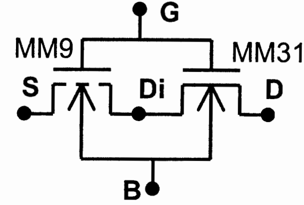

Fig. 2. The macro model used for DC–characterization.

4 Self-Heating

Due to considerable power dissipation and the low thermal conductive box layer, the temperature in the device rises significantly. Analysis of the one-dimensional heat flow shows that the temperature rise ΔT in the device due to self-heating is given by

$$\Delta T = R_{th} I_{DS} V_{DS}\,, \qquad R_{th} = \frac{t_{box}}{k_{box} A_{box}}, \tag{1}$$

provided that heat loss in the Si-substrate is neglected. Here, k_{box} = 1.4 Wm/K is the thermal conductivity of oxide, and $A_{box} = W_{box}L_{box}$ is the area of the box layer. The thermal resistance R_{th} is extracted from the DC-conductance, by incorporation of temperature scaling rules according to

$$X|_{T+\Delta T} = X|_T + S_X \Delta T \qquad \text{or} \qquad X|_{T+\Delta T} = X|_T \left(\frac{T}{T+\Delta T}\right)^{\eta_X}, \tag{2}$$

for a temperature-dependent parameter $X|_T$ at a given ambient temperature T. Here, $X|_{T+\Delta T}$ denotes the parameter corrected for self-heating, and η_X, S_X are the temperature coefficients.

5 LDMOS Extraction Strategy

For a set of devices of widths W varying from 5 μm to 114 μm, gate lengths L between 1 and 2 μm (the channel length is fixed by the p-well diffusion) and temperatures T between 10 and 125 °C, the model parameters are extracted according to the following strategy:

1. Assuming η_X and S_X, one evaluates at temperature T the model including self-heating, and extracts the parameters $X|_T$.
2. By executing step 1 at various T-values, the temperature coefficients η_X and S_X can be determined.
3. Repeat step 1 and 2 in an iterative procedure, until the temperature coefficients found in step 2 correspond to those used in step 1.

4. Extract for a reference temperature the parameters for various widths W, and determine the width scaling rules.
5. Extract the parameters for various gate lengths L, and determine the length scaling rules for the drift region.

These temperature and device scaling rules are subsequently used to determine the current at a certain temperature and device dimension.

6 Results

In Fig. 3 the effect of self-heating is shown by a reduction of the conductance in the saturation regime. For a lower temperature this effect is more pronounced. Fig. 4 shows the increase of the thermal conductance $1/R_{th}$ with box width W_{box}. We observe that, due to two-dimensional effects, the extracted values deviate slightly from the linear trendline predicted by (1) with $A_{box} = W_{box}L_{box}$. The slope of this trendline predicts a thermal conductance k_{box} of 1.3 Wm/K, which corresponds reasonably to the theoretical value of 1.4 Wm/K.

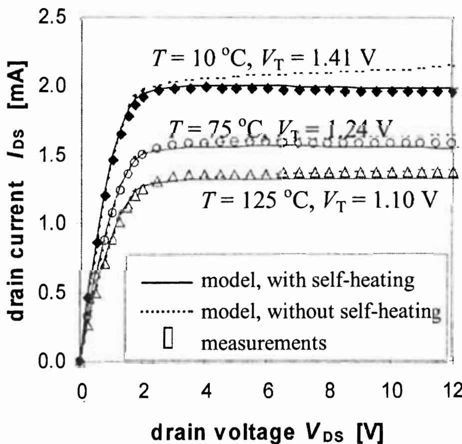

Fig. 3. The effect of self-heating for W = 17 μm, L = 1.6 μm and $V_{GS} = V_T + 3.1$ V.

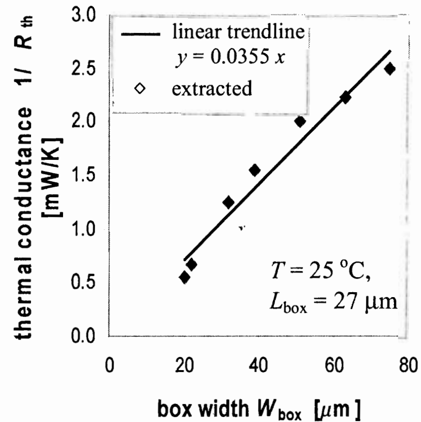

Fig. 4. The extracted thermal conductance $1/R_{th}$ and the linear trendline corresponding to (1).

Figs. 5 and 6 show, for grounded Si-substrate and p-well contact, measured DC-data and modelled results for larger device widths. Fig. 5 shows the drain current and transconductance g_m versus gate voltage. Here, a temperature rise ΔT due to self-heating of up to 110 °C is reached. Fig. 6 shows the drain current and conductance $|g_{DS}|$ versus drain voltage. The self-heating effect is clearly shown by a negative output conductance. In contrast to [2], where the effect of self-heating is due to a decrease in the conductance of the drift region, here the effect of self-heating is mainly caused by a decrease in the conductance of the *channel*.

7 Conclusions

By use of the macro model consisting of MM9 for the channel and MM31 for the drift region, an LDMOS transistor in SOI has been characterized accurately over a wide range of dimensions, temperatures and bias conditions. The effect of self-heating has

been found to be significant, and needs to be incorporated during parameter extraction. Incorporation of self-heating has led to a physics based model that accurately predicts the SOI-LDMOS characteristics. The model is successfully used in high-voltage IC-design.

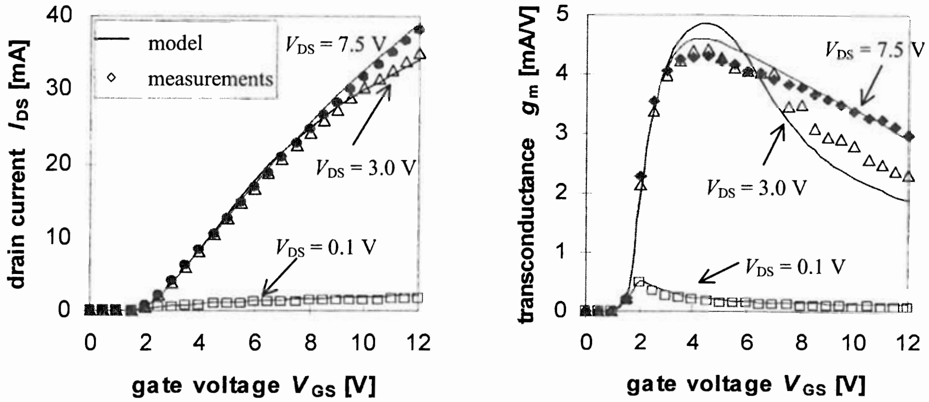

Fig. 5. The measured and simulated drain current and transconductance, for $W = 114$ µm, $L = 1.6$ µm and $T = 25$ °C.

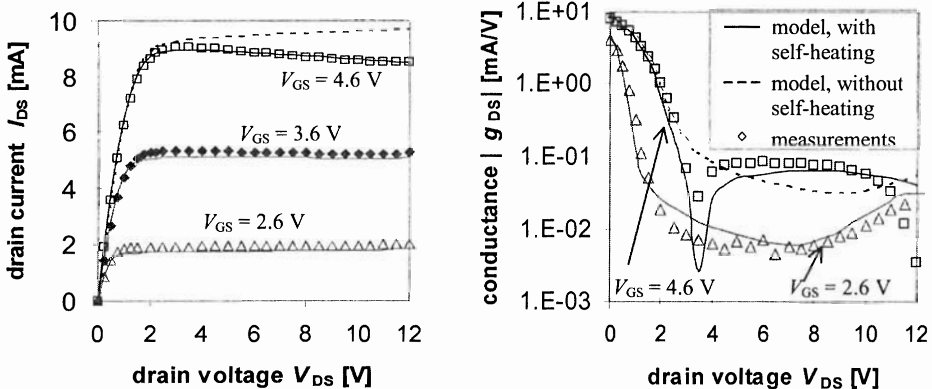

Fig. 6. The measured and simulated drain current and conductance, for $W = 90$ µm, $L = 1.6$ µm and $T = 25$ °C.

References

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