Development of an Optimised 40V pDMOS Device by Use of a TCAD Design of Experiment Methodology

P. Moens[1], M. Tack[1], H. Van hove[1], M. Vermandel[2] and D. Bolognesi[1]
[1]Alcatel Microelectronics, Westerring 15, B-9700 Oudenaarde, Belgium.
[2]TFCG/ELIS, University of Ghent, StPietersnieuwstraat 41,B-9000 Ghent, Belgium
E-mail : peter.moens@mie.alcatel.be

Abstract : **A new medium voltage (40-60 V) pDMOS device has been developed and optimized through the use of a Design of Experiment (DOE) approach based on TCAD simulations and experimental verification. Layout parameters are varied and the electrical characteristics of the device (e.g. Vbd, specific on-resistance, ...) together with hot carrier behaviour, are studied as responses. In this way, an optimal device was selected.**

I. Introduction

Smart power technologies, integrating high voltage devices with standard low voltage CMOS cores, have found several applications in e.g. automotive and telecommunication products [1-5].

Alcatel's I^2T technology [6] (Intelligent Interface Technology) has been designed to allow applications up to 100V. It is based on a 0.7μm analogue CMOS technology with the addition of 100V n/pDMOS and 80V NPN/PNP BJTs. The high voltage modules are realised by a modular approach adding several additional masking steps i.e. N-type buried layer, deep Ntub, selective Pwell, self-aligned PBody (for nDMOS) and double poly (allowing two gate oxides of 17 and 42 nm). However in quite some applications maximum voltages of no more than 40V-60V are required, thus allowing much smaller devices than the existing 100V devices.

This paper describes the development of a new pDMOS device in the I^2T technology, that is optimised for medium voltage (40-60V) applications. Development of optimal DMOS devices is a complex process, where several device-design parameters should be taken into account, and where simultaneous optimisation is needed towards maximum breakdown at minimal Ron, minimum area, high reliability performance, and ideal output characteristics. Extensive use of DOE matrices, based on TCAD simulations are done. The results obtained are verified on silicon and an explanation of the observed features is given. In this way, the time-to-market of additional devices in an existing technology can be greatly reduced.

II. Device Description

Fig. 1 shows a cross-section of the new pDMOS device. It uses a 42 nm gate oxide, the Nwell/Pwell regions of the basic 0.7 μm CMOS technology are used as channel/drift regions, and the whole structure is isolated through the use of Nwell/Ntub/N-type Buried layer. The main device-design parameters to be optimised are indicated : the channel length X, the thin oxide gate controlled drift region Y, the field oxide controlled drift region Z and the field oxide length T.

III. DOE Description and Results.

The DOE approach is based on the following steps:

(1) Screening simulations of all design parameters X, Y, Z, T (see Figure 1).
(2) Full matrix simulations of the main parameters, and selection of the experimental conditions.
(3) Processing and characterisation of a matrix of real silicon devices.
(4) Selection of the optimal device and comparison with the TCAD data.

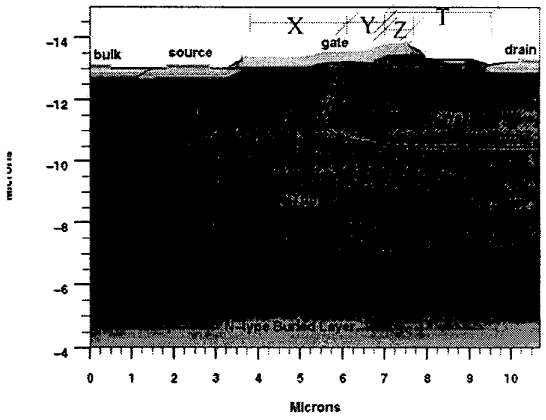

Fig. 1 : cross-section of the pDMOS device

0-7803-6279-9/00/$10.00 © 2000 IEEE

Extensive use is made of TCAD tools for steps (1) and (2), and in order to understand some of the observed behaviour. Out of step (1), the main design parameters are deduced. For the most important parameters, a DOE is set up with response parameters Ron, Vbd, Vt, transconductance, Idsat and hot carrier degradation.

From screening simulations, it turned out that Y, and to a lesser extent X, are the most important design parameters to be tuned. Indeed, these parameters greatly influence the position of the Pwell/Nwell junction with respect to the birds beak under the gate oxide. T and Z merely determine the minimum achievable value for the breakdown voltage. From first simulations, T and Z are fixed to 3.0 μm and 1.0 μm respectively. Larger T values will increase the Ron. Due to Vt roll-off, a minimum value for X of 2.0 μm is obtained.

Thus, full matrix simulations are performed for the X and Y design parameters. The response surfaces for breakdown voltage (Vbd) and specific on-resistance (Ron) are shown in Figs. 2 and 3 respectively. The pDMOS breakdown Vbd (at Vg=0.0 V) decreases monotonously (in absolute value) with increasing Y. This is explained by the Nwell/Pwell junction curvature due to the growing impact of the gate with increase in Y. X does not have a large impact on the breakdown voltage.

The specific on-resistance Ron (defined as Vd/Id at Vd=-0.5V for Vg=-12V), is slightly decreasing for decreasing Y due to the decrease in drift region length. See Fig. 3. Ron is going through a minimum at Y=0.5 μm, and strongly increases for smaller Y. The latter also results in non-saturation of the output characteristics at higher Vg, a behaviour which is difficult to model with present available DMOS models and is a problem in many applications. Fig. 4 shows simulated output characteristics for Y=0.0 μm and Y=1.0 μm, clearly indicating the non-saturating behaviour at high Vg, for Y=0.0 μm.

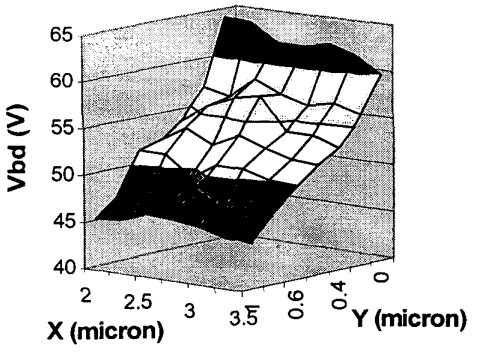

Fig. 2 : Response surface for the breakdown voltage

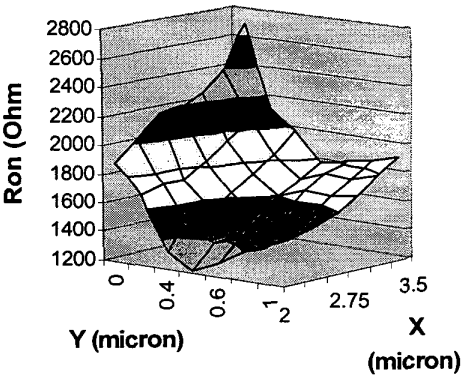

Fig. 3 : Response surface for the specific on-resistance (Ron)

The non-saturating behaviour and the high Ron for low Y values can be explained by looking at Figs. 5 and 6, showing the current flow at Vg=-12V, Vd=-45V, for a device with Y=0.0 μm and Y=1.0 μm respectively. For Y=1.0 μm, the current flows from the inversion channel (Nwell) into an accumulation channel (Pwell) that is pinched off under the gate oxide, and is then widely spreading out into the drift region. This results in a low Ron and good saturation characteristics. On the contrary, for Y=0.0 μm, the current flows from the inversion channel into a narrow high resistive path under the field oxide, before spreading out. Indeed, since the gate control under the field oxide is weak, only a weak accumulation channel is built. As the junction is located under the field oxide, the Vt increases slightly for Y=0.0 μm (approximately 10 %).

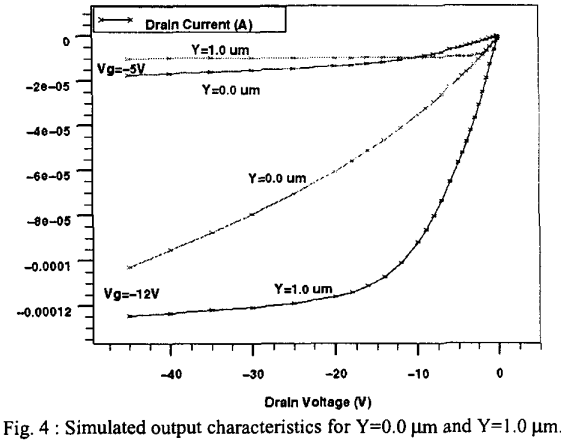

Fig. 4 : Simulated output characteristics for Y=0.0 μm and Y=1.0 μm.

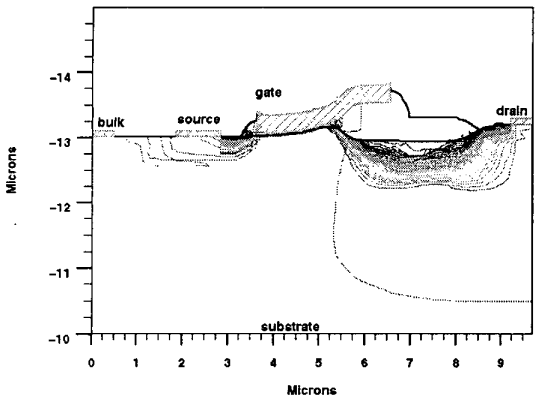

Fig 5 : Simulated current flow for Y=0.0 µm (Vg=-12V, Vd=-45V)

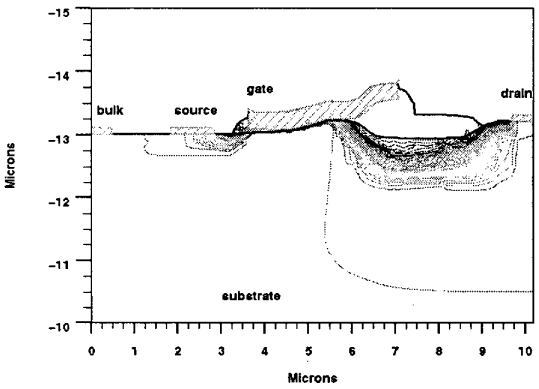

Fig 6 : Simulated current flow for Y=1.0 µm (Vg=-12V, Vd=-45V)

In addition reliability simulations have been performed for different X and Y dimensions. The stressing conditions are Vg=-12V and Vd=-45 V. Simulated data are collected after stressing the device for 1E4 s. The results for the degradation of e.g. Ron are plotted in Fig. 7. Similar graphs are obtained for the degradation of the other electrical parameters. It follows that for small Y values (Y <0.2 µm), the Nwell/Pwell junction is located under the birds beak. As simulations indicate that the maximum value of the impact ionisation occurs very close to the field oxide interface, hot carriers will be injected into the field oxide. These injected electrons shift the junction under the channel thus improving the device performance : Vt is slightly decreased, transconductance is increased, Ron is decreased and Vbd is increased. In addition, the saturation characteristics are improved.

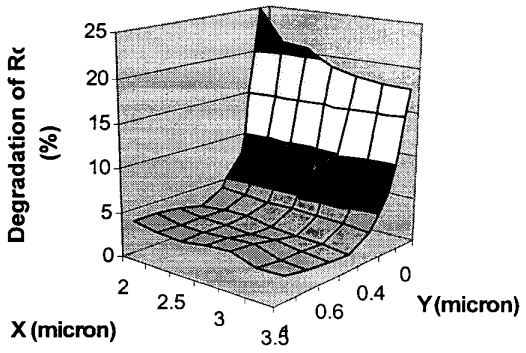

Fig 7 : Response surface for the degradation of the specific on resistance.

In order to choose the optimum device layout out of the TCAD simulations, an empirical figure of merit (FOM) is calculated according to (1) :

$$FOM = Vbd/(Ron*pitch*degradation) \qquad (1)$$

This empirical formula will favour a device with a high Vbd, low Ron, low degradation and small pitch (the pitch is defined as the distance between the centre of the bulk contact and the centre of the drain contact). However, devices with a breakdown voltage less than 45 V (in absolute value) are rejected, because a minimum voltage of 40V is required and due to possible process variations (e.g. misalignments), a minimum safety margin of 5V has to be allowed for.

The evaluation of the figure of merit for varying X and Y is shown in Fig. 8. As indicated above, no simulations for X < 2 µm have been performed due to Vt roll-off for smaller X values. From Fig. 8, it follows directly that the optimum values for X and Y are 2.0 µm and 0.5 µm respectively. For this device, Vbd is high enough (52 V), degradation is low, Ron and pitch are acceptable. For larger X values, the breakdown voltage of the device increases, but also the pitch and the on-resistance increase.

In conclusion, from TCAD simulations the following layout of the optimum device is proposed : X=2.0 µm, Y=0.5 µm, Z= 1.0 µm and T=3.0 µm.

IV. Experimental Verification

Based on the above TCAD study, a variety of pDMOS devices, with varying X, Y, Z and T, are designed and processed in the standard I^2T technology. Special attention is paid to the layout variations for X and Y.

A comparison between simulated and experimental data for different Y values is depicted in Fig.9. The

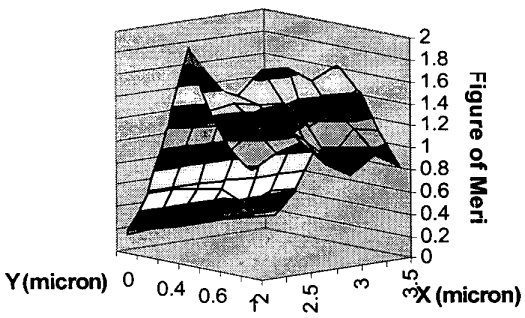

Fig. 8 : Response surface for the figure of merit calculated according to (1).

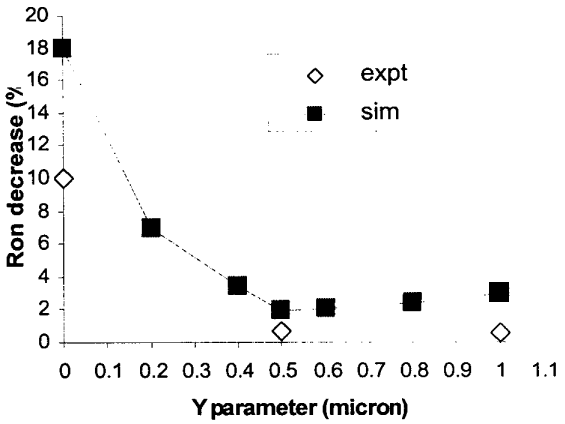

Fig 10 : Comparison between simulated and experimental data for the degradation of the specific on-resistance (Ron).

correspondence for the breakdown voltage is very good. For the specific on-resistance, the simulated values seem to be somewhat overestimated. This is most probably due to a poorly calibrated device simulation parameter. However, the observed tendencies correspond very well to the simulated ones (minimum obtained for Y=0.5 μm).

Finally, a comparison between measured and simulated degradation of the specific on-resistance is depicted in Fig. 10. Again the observed tendencies agree very well with the TCAD simulations. The main conclusions as predicted by TCAD are confirmed by experimental evidence.

Thus, it can be concluded that the best device as predicted by TCAD simulations is the same as the one processed on silicon.

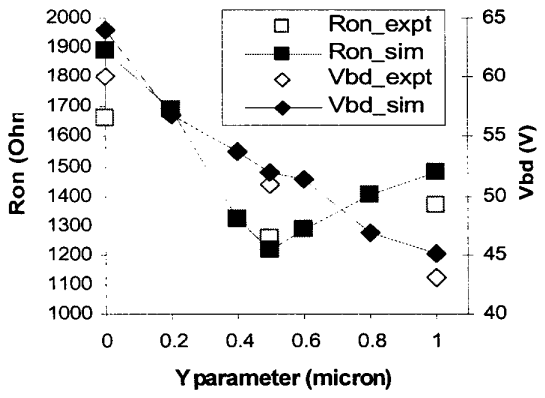

Fig 9 : Comparison between simulated and experimental data for Ron and Vbd

V. CONCLUSIONS

Optimisation of the various pDMOS device-design parameters is reached through the use of DOE techniques both by TCAD simulation and experimental verification.

Simulation of the electrical response of the devices and their reliability behaviour as a function of the most critical design parameters is in very good agreement with experimental data. Hence, it is proven that by using TCAD, a lot of information about the electrical and reliability behaviour of the pDMOS device can already be gathered before any silicon is processed. In this way, the time-to-market for a given series of devices in a well-known technology is strongly reduced.

REFERENCES

[1] B.J. Baliga, "Trends in Power Semiconductor Devices", *IEEE Trans. Electron Devices*, vol 43, pp1717-1731, October 1996.

[2] C. Contiero et al., "Trends and Issues in BCD Smart Power Technologies", *ESSDERC*, pp111-118, September 1999.

[3] M.I. Castro-Simas et al., "Smart Power in MOS Technologies – An Overview", *ISIE*, pp371-387, 1997

[4] C. Contiero, P. Galbati, M. Palmieri, G. Ricotti, R. Stella "Smart Power Approaches VLSI Complexity", *ISPSD*, pp11-16, 1998.

[5] S. Mukherjee "Power integrated circuit : progress, prospects and challenges", *IEEE Trans. on Electron. Devices*. vol 36, pp2599-2604, November 1989.

[6] D. Wojciechowski, A. Van Calster and J. Witters, "TCAD Applied to the Development of DMOS Devices", *ISDRS*, pp 785-788, 1995.