A High Signal Swing Pass-Transistor LogicUsing Surrounding Gate Transistor

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Abstract-**In this paper a pass-transistor logic (PTL) using Surrounding Gate Transistor (SGT) is reported for the first time. This SGT-based PTL brings out the latent abilities of the PTL, especially improvement of the area occupation by 74% and the power-delay product by 70% at the supply voltage of 1V compared to bulk MOSFET-based PTL.**

I. INTRODUCTION

Recently, with the rapid scaling of LSI's, it has been indispensable to minimize power dissipation. On this background, research about PTL, which is the logic style that has capability to achieve high-speed, low-power and small area occupation at the same time, are widely done [1]. However, PTL has not succeeded in capturing a mainstream logic style yet. It is caused by the inferior characteristics of the mainstream device, the bulk MOSFET. These are body-effect, small signal swing and current capability, poor subthreshold swing, large junction capacitance and large transistor size. These characteristics lower logic operation speed, operation stability and the performance at low supply voltages. Therefore, we propose in this paper a pass-transistor logic based on the SGT [2,3] structure. The SGT-based PTL achieves higher signal swing and current capability, smaller static leak current, lower load capacitance and parasitic resistance in comparison with bulk MOSFET-based PTL. The SGT-based PTL overcomes the difficulty in achieving higher speed operation, lower power dissipation and smaller area occupation at low supply voltages at the same time.

II. SURROUNDING GATE TRANSISTOR

Figure 1 shows the structure of SGT used in the SGT-based PTL. Channel region is floating and SGT is body-effect free [4]. By this, SGT-based PTL can basically dissolve the reduction of the signal swing and the current capability. Moreover, the surrounding gate increases the current capability of pass-transistor due to the concentrated gate electric field. The vertical structure of SGT contributes to the smaller area occupation and lower junction capacitance. Under these circumstances, SGT is suitable for pass-transistor logic with high-speed operation and stable logic operation at low supply voltages.

III. EXTRACTION OF MODEL PARAMETER FOR SGT

In this paper, for the evaluation of the SGT-based PTL, SPICE was used. Model parameters of SGT are extracted from SGT I-V characteristics of the three-dimensional device simulation.

IV. RESULT AND DISCUSSION

Figure 2 compares the signal swing of the SGT-based pass-transistor and bulk MOSFET-based pass-transistor. The threshold voltage of both SGT and bulk MOSFET equals 0.4 V. The high-level output signal drop of bulk MOSFET pass-transistor is greater than 0.4 V due to the an increase of threshold voltage with body-effect. The voltage drop of the high level output signal of SGT nearly equals 0.4 V because there is no body-effect. As a result, the high-level output signal of SGT is improved by 25% compared to bulk MOSFET.

A 3 × 3 full adder array is used to evaluate the performance of the SGT-based PTL. Figure 3 shows the PTL 1b-full adder circuit. Figure 4 shows the layouts of PTL 1b-full adder circuits constructed by SGT and bulk MOSFET with 0.2 m rule, respectively. Transistor width ratio of nMOS and pMOS in the buffer are optimized to obtain the best performance. The full adder circuit area of the SGT-based PTL (14.625 m^2) is reduced by 74 % compared to the one of the bulk MOSFET-based PTL (55.897 m^2). This is because SGT is smaller compared to a bulk MOSFET having the same gate width. Figure 5 shows the contributions to the load capacitance of full adder for the SGT- and the bulk MOSFET-based PTL. Because the SGT-based PTL can reduce junction capacitance by 88%, total load capacitance of full adder is reduced by 51% compared to bulk MOSFET-based PTL. Figure 6 shows the dependence of the full adder delay time on supply voltage for the SGT- and the bulk MOSFET-based PTL. The SGT-based PTL can improve the operation speed within the whole range of supply voltage. Compared to the bulk MOSFET-based PTL, the increase of the delay time at low supply voltages is suppressed because the SGT-based PTL is body-effect free, and has a higher current capability combined with lower load capacitance and resistance. Compared to bulk MOSFET-based PTL, the delay time of the SGT-based PTL is improved by 26% at a supply voltage of 2V, and by 48% at 1V, respectively. Figure 7 shows the dependence of the full adder power-delay product on supply voltage for the SGT- and the bulk MOSFET-based PTL. Compared to bulk MOSFET-based PTL, the power-delay

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product of the SGT-based PTL is improved by 45% at a supply voltage of 2V, and by 70% at 1V, respectively. Compared to bulk MOSFET, using SGT reduces the supply voltage which is necessary to obtain a minimum in the power-delay product (from 1.4 V to 0.8 V). The minimum power-delay product of the SGT-based PTL at the supply voltage of 0.8 V is improved by 68 % compared to one of bulk MOSFET-based PTL at 1.4 V.

V. Conclusion

The proposed SGT-based PTL improves area occupation, delay time and power-delay product by 74%, 48%, 70% respectively at the supply voltage of 1V compared to bulk MOSFET-based PTL, and overcomes the demerits of bulk MOSFET-based PTL. As a result, the SGT-based PTL is one of the candidates to overcome the problem which CMOS LSI's have been faced.

References

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[4] H. Takato, et al., "Impact of surrounding gate transistor (SGT) for ultra-high-density LSI's," IEEE Trans. ED, vol. 38, p.573, 1991.

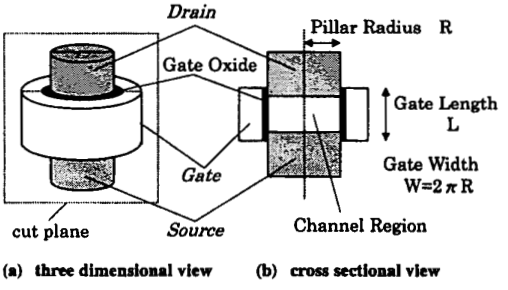

Figure 1: Structure of Surrounding Gate Transistor.

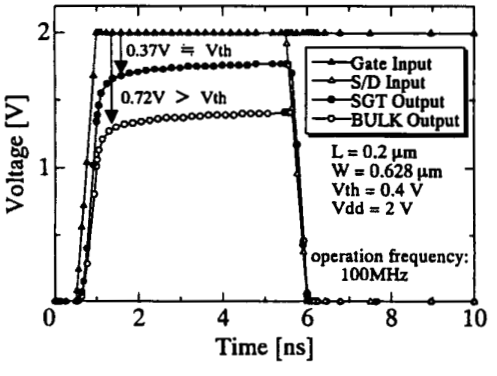

Figure 2: Signal swing of SGT and bulk MOSFET pass-transistor.

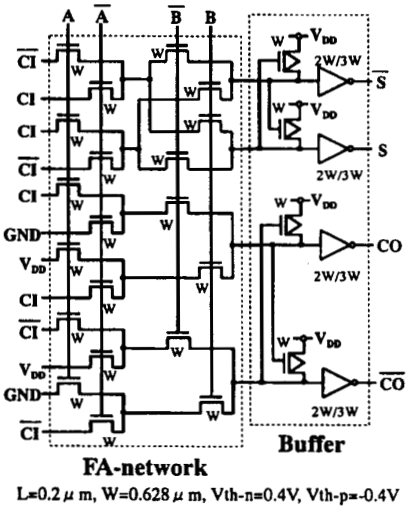

Figure 3: 1b-full adder circuit.

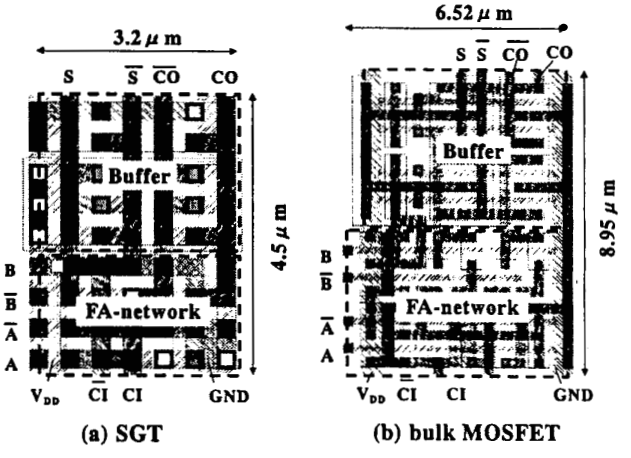

Figure 4: 0.2 μ m rule layout of full adder.

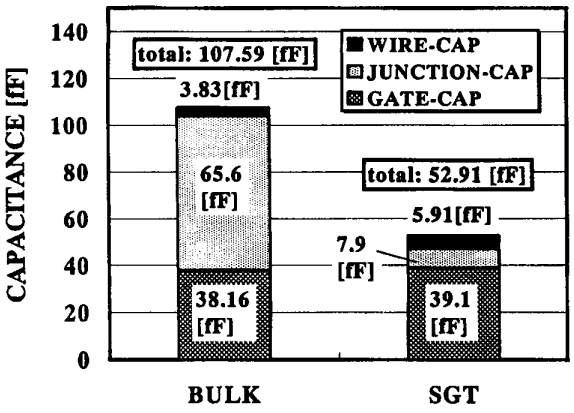

Figure 5: Contributions to the load capacitance of full adder.

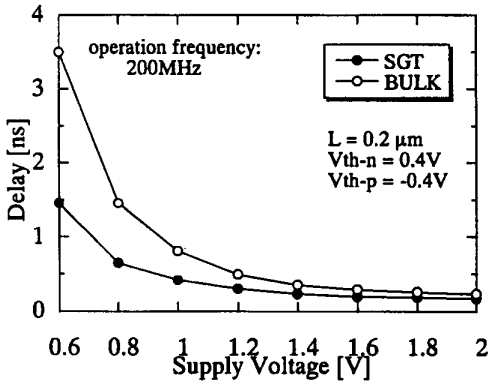

Figure 6: Full adder delay dependence on supply voltage.

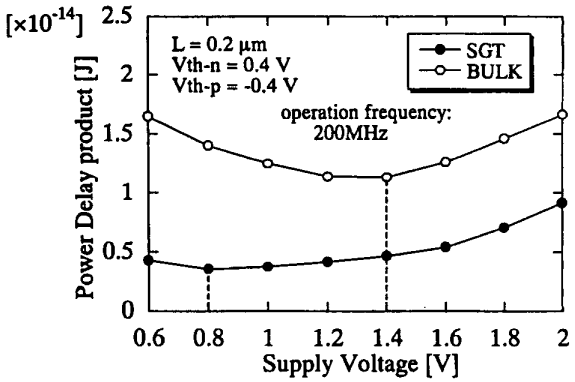

Figure 7: Full adder power delay product dependence on supply voltage.