Simulation of Multiple-Bit Soft Errors Induced by Cosmic Ray Neutrons in DRAMs

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***Abstract*—Although it has been shown that cosmic ray neutrons play an important role in soft error (SE) phenomena, some important issues to clarify in neutron-induced SE phenomena are remained. In this paper, neutron-induced multiple-bit SEs in 16Mb DRAMs are investigated numerically using Neutron-Induced Soft Error Simulator, NISES, and simulated results are compared to experimental data. Scaling effects on multiple-bit SEs, effects of configuration patterns on double-bit SE rates, and the influence of multiple-bit SEs on an error correction code are discussed.**

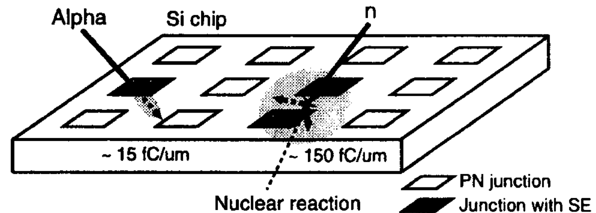

Fig. 1. Neutron-induced multiple-bit SEs.

I. Introduction

Cosmic rays, especially neutrons, can induce soft errors (SEs) in digital electronics at sea level [1]. While it has been shown that neutrons play an important role in SE phenomena for memory circuits [2]-[10] and logic circuits [7]-[9], some important issues to clarify in neutron-induced SE phenomena are remained. The multiple-bit SE [2] [3] [10] is one of important issues in neutron-induced SE phenomena to clarify.

In DRAMs that are made with recent technologies, the soft error rates (SERs) due to α-particles are very small and multiple-bit SERs due to α-particles are negligible. However, because the cosmic ray neutrons induce a large number of charges in a silicon medium through nuclear reactions, they can induce multiple-bit SEs (Fig. 1). In this paper, we focus on the neutron-induced multiple-bit SEs in DRAMs

The numerical approach is important for neutron-induced SEs, because we cannot easily carry out neutron-accelerated testing or cosmic ray neutron field testing. Neutron-accelerated testing needs a high-energy neutron or proton beam [4]-[6] and cosmic ray neutron field testing is time consuming [2] [3]. We have developed Neutron-Induced Soft Error Simulator (NISES) [11] [12] and applied it for analysis of neutron-induced SEs. In this work, we extended NISES for analysis of multiple-bit SEs and applied it for multiple-bit SEs in DRAMs. We discuss characteristics of neutron-induced multiple-bit SEs, i.e., scaling effects on multiple-bit SEs, effects of configuration patterns on double-bit SE rates, and the influence of multiple-bit SEs on an error correction code (ECC) and show their significance in VLSI technologies.

II. Neutron-Induced Soft Error Simulator

NISES [11] [12] contains a database both for the neutron-nucleus reaction and for the electron-hole pair generation. Antisymmetrized Moleculer Dynamics (AMD) [13] [14] [15] which is recently proposed nuclear reaction theory forms the foundation of the nuclear reaction database . NISES simulates charge collections induced by reaction products with the Monte Carlo procedure. If the charges induced in the sensitive volume pass a critical charge, we assumed that an SE occurs.

For analysis of multiple-bit SEs, we assumed an array of PN junctions (or sensitive volumes, Fig. 2). If the charges in two (or greater than two) sensitive volumes pass a critical charge simultaneously with the same reaction, a multiple-bit SE occurs. To avoid an increase of the simulation time, we included a periodic boundary condition for an array of PN junctions (Fig. 2).

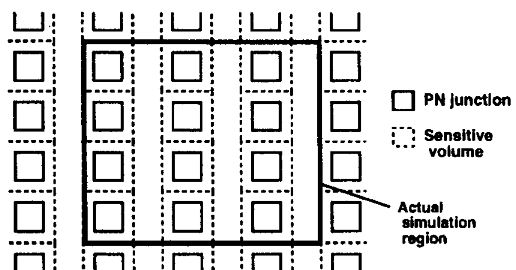

Fig. 2. PN junction array and periodic boundary condition.

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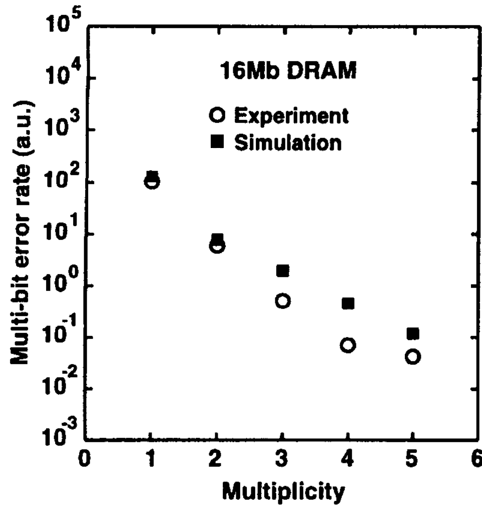


Fig. 3. Measured and simulated multiple-bit SERs in 16Mb DRAMs.

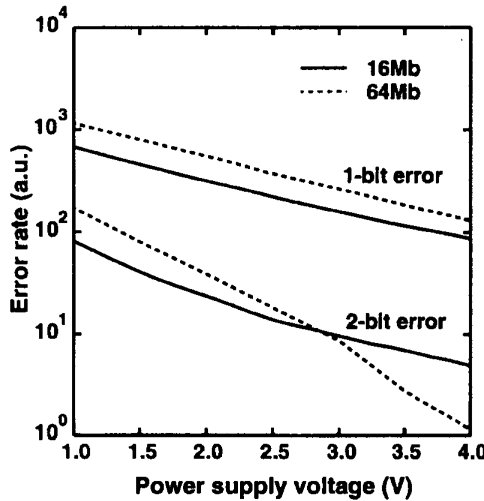


Fig. 4. Simulated neutron-induced SERs as a function of the power supply voltage.

III. Results and discussions

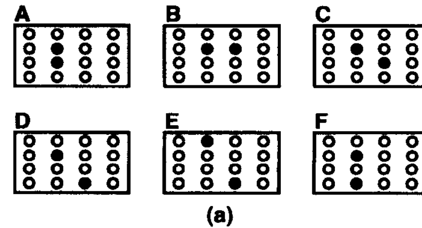
Figure 3 shows the simulated and measured neutron-induced multiple-bit SERs of 16Mb DRAMs. The experiment was performed at the Los Alamos National Laboratory. A pulsed neutron beam having an energy spectrum similar to the sea-level atmospheric neutron energy spectrum was used [9]. In the experiment, prototype 16Mb DRAM chips by Fujitsu, which were made with stacked capacitor technology, were arranged in an array perpendicular to the beam direction. The maximum multiplicity in measured multiple-bit SEs was five. As the multiplicity increase one, multiple-bit SER decreases to about 1/10. The simulated neutron-induced multiple-bit SERs of 16Mb DRAMs agreed with measured data (Fig. 3).

Table 1. Scaling law of neutron-induced SERs.

Factor for next generation	1-bit (Sim.)	2-bit (Sim.)
Cell area (x 0.5)	x 0.41	x 0.14
Power supply voltage (x 0.7)	x 1.74	x 4.33
bit number (x 4)	x 4	x 4
SER/chip	x 2.8	x 2.4

To investigate the scaling effects, we simulated the multiple-bit SEs in 64Mb DRAMs (Fig. 4). As the supply voltage decreases, the 1-bit SE curve of 64Mb DRAMs has a similar slope with that of 16Mb DRAMs, but the 2-bit SE of the 64Mb DRAMs increases more rapidly than that of 16Mb DRAMs. The scaling law of neutron-induced SERs was summarized in Table 1. 2-bit SERs decreases more rapidly as the cell area decreases than 1-bit SERs, but they increases more rapidly as the power supply voltage decreases than 1-bit SERs. It suggest that the multiple-bit SEs may increases as the power supply voltage decreases drastically in the future generation of DRAMs.

Double-bit SERs of 6-type configuration patterns in multiple-bit SEs were investigated and it was found that the double-bit SER decreases as the distance between the storage nodes increases and, on a logarithmic scale, this



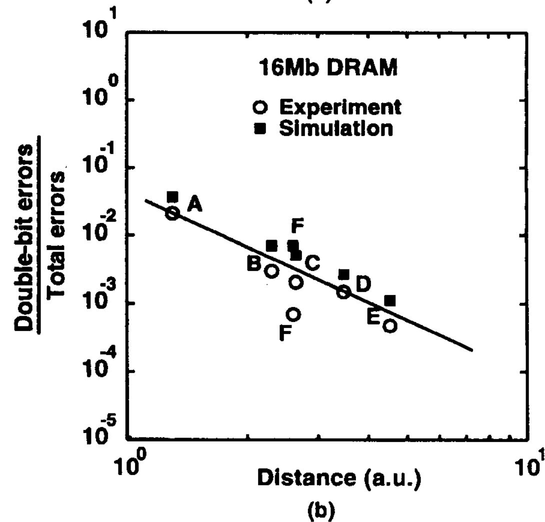


Fig. 5. Double-bit SERs for 6 types of configuration patterns.

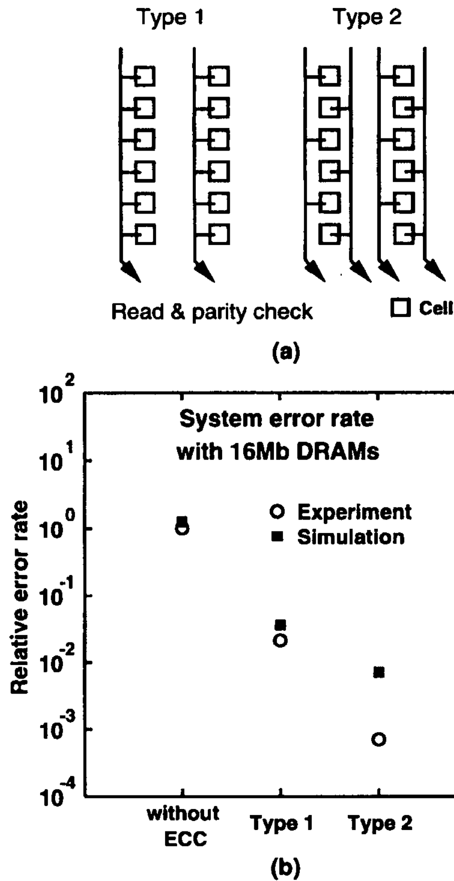


Fig. 6. Neutron-induced error rate in system with ECC.

variation appears to be linear (Fig. 5).

An error correction code, ECC, is often used to suppress SEs in high reliability computer systems. We examined the error rates in systems that used two types of ECC, (Type 1 and Type 2, Fig. 6). In Type 1, all bits in the same row are read simultaneously. If the information of a single bit changes, the SE is corrected. However, if two bits in the same row fail simultaneously, the SEs are not corrected. In type 2, all every other bit in the same row are read simultaneously. In this case, two SEs of bit-neighboring are corrected, but two SEs of bit-skipping are not corrected. Fig. 6 show the neutron-induced error rates in a system that uses ECC. The error rates for Type 1 are 4.0 - 8.0 % of the error rate without ECC and the error rates for Type 2 are 0.1 - 1.0 % of the error rates of without ECC. These results prove therefore cosmic ray neutrons can induce errors even if an ECC of Type 1 or 2 is used in the system.

In the future generation of DRAMs, the multiple-bit SEs may increases as the power supply voltage decreases. Consequently, an accurate estimation of multiple-bit SEs will be important for the ECC design which properly suppress multiple-bit SEs in high reliability systems.

IV. Conclusion

Characteristics of neutron-induced multiple-bit SEs in DRAMs were investigated using our simulator NISES. Scaling effects on multiple-bit SEs, effects of configuration patterns on double-bit SERs, and the influence of multiple-bit SEs on an ECC were discussed. Our results suggest that the multiple-bit SEs may increases as the power supply voltage decreases in the future generation of DRAMs. We also shown the significance of multiple-bit SEs for the ECC design. Consequently, an accurate estimation of multiple-bit SEs will be important for the ECC design which properly suppresses multiple-bit SEs in high reliability systems.

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