Quantum-Mechanical 2D Simulation of Surface- and Buried-Channel p-MOS

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Abstract— **A two-dimensional MOS device simulator including quantum-mechanical effects has been developed and applied to surface- and buried-channel p-MOS devices. The Schrödinger equation is solved retaining a large number of eigenstates, which are then used to build a modified classical distribution accounting for the high energy part of the distribution. With this approach, discontinuities in the gate capacitance near flat bands have been eliminated without introducing any empirical parameter. For accurate device simulation, experimental data on the hole mobility were collected, and a non-local mobility model was used for carriers in the bound levels. A standard mobility model is adopted instead for the classically-distributed carriers. Results are presented for the gate capacitance and drain current of 0.35 μm devices, showing a good agreement over a wide range of channel doping concentrations.**

I. Introduction

Modeling of channel quantization has become a key issue in ULSI device simulation, due to its strong impact on device characteristics like threshold voltage, on-state current and gate capacitance [1, 2]. Until recently, however, efforts have been mainly devoted to one-dimensional (1D) simulations of n-channel devices, due to either their higher importance when compared to p-MOSFETs and to the simpler structure of the conduction band. As a result, few attempts to address the problem of valence band quantization can be found in the literature [2–4].

Moreover, whenever device simulation is used to accurately assess the targets and tradeoffs in scaled device design, two-dimensional (2D) quantum-mechanical (QM) simulations are required, resulting in a formidable computational task. Although approximate solutions have been developed [5, 6], only recently the problem of 2D QM simulation of n-MOSFETs has been tackled [7].

In this work, 2D QM simulation of p-MOSFETs is addressed, extending a previous numerical model developed for n-MOS devices [8]. Discontinuities in the simulated capacitance near flat bands are eliminated and a non-local mobility model is adopted in the inversion layer. Simulation results are compared against $I-V$ and $C-V$ experimental data, showing a good agreement over a wide range of channel doping concentration for both surface- and buried-channel devices.

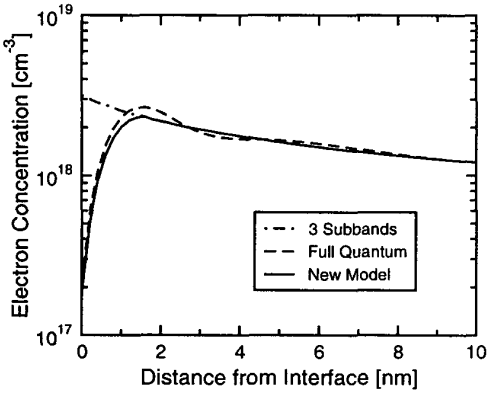

Fig. 1. Electron concentration in a p-MOSFET biased near flat bands calculated with the different models. Note that, as no levels are bound, the 3-subbands approach returns a purely classical solution.

II. Carrier Quantization Near Flat Bands

In our approach, the 1D Schrödinger equation is solved along several sections inside a "quantum box" region, including the inversion channel as well as part of the source/drain regions. The solution is then interpolated in the direction parallel to the silicon/oxide interface [7]. Full 2D solutions are instead retained for the Poisson and continuity equations. The model is expected to be reliable until the channel length becomes comparable to the electron wavelength, thereby forcing a full QM treatment [9]. In our simulations, the vertical depth of the quantum box region could be varied between 10 nm and 40 nm without a significant modification of the overall charge density.

A smooth transition between the quantum box and the remaining classical regions is typically obtained using the so-called three subbands approach [10]. After solution of the Schrödinger equation, up to three bound levels are actually populated with carriers according to the 2D density of states. To describe the carrier distribution at higher energies, a classi-

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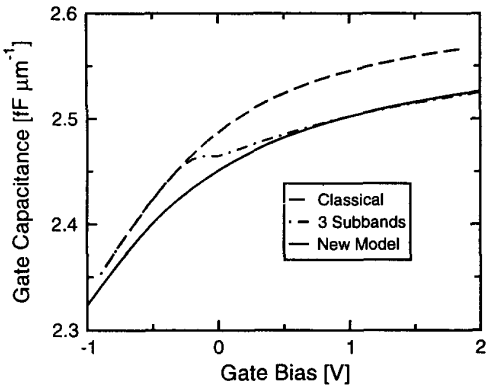

Fig. 2. Simulated gate capacitance near flat bands for the same device as in Fig. 1.

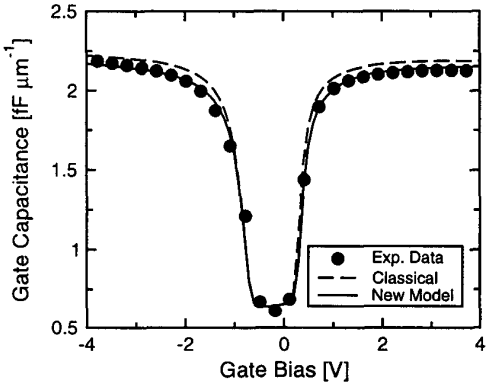

Fig. 3. Gate capacitance for the buried-channel device, according to the classical and new QM models.

cal "tail" distribution is added, starting from the fourth or the last bound level [10, 11]. This approach works well in strong accumulation or inversion, *i.e.*, when there is at least one bound level in the potential well, but is well known to cause numerical instabilities near flat bands. The reason for such instabilities can be seen in Fig. 1, where the electron concentration in a *p*-MOS device biased near flat bands is shown. As the last bound level becomes free, the three-subbands approach switches from a QM to a purely classical solution, dramatically changing the charge distribution. This leads to a strong sensitivity of the charge distribution to the potential, hence to numerical instabilities. To overcome this issue, empirical approaches based on approximate expressions for the quantized charge, have been developed [5, 12].

On the other hand, as a consequence of the existence of an abrupt energy barrier at the silicon/oxide interface, QM effects can be seen in the charge distribution even when no confinement takes place. In fact, the real QM solution always vanishes at the interface, leaving a so-called "dark space" depleted

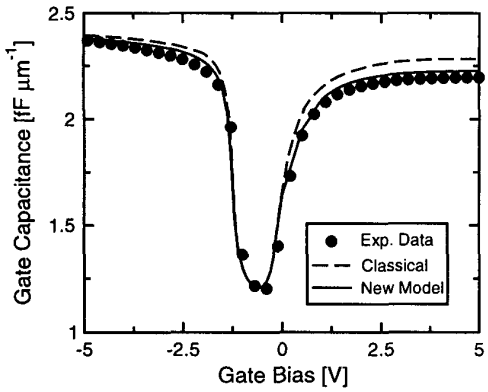

Fig. 4. Gate capacitance for the surface-channel p-MOS device with peak channel doping of 7.3×10^{16} cm^{-3}.

of free carriers [13]. This region has a thickness of the order of the de Broglie hole wavelength. It follows that discontinuities in the charge distribution can be eliminated if the real QM solution is retained in all bias conditions. In our approach, the Schrödinger equation was solved using a large number of eigenstates, always obtaining the correct charge distribution. Parameters for the valence band were taken from [2]. To retain a smooth transition between the quantum box and the remaining fully-classical regions, we followed a three-subbands approach, populating up to three bound levels with the QM charge and adding a "tail" distribution, n_t. However, to reproduce the real QM distribution, the tail was obtained modulating the purely classical distribution n_{CL} by the full QM charge n_{QM} as

$$n_t(x) = n_{CL}(x)\frac{n_{QM}(x)}{n_{QM}(x_p)}, \tag{1}$$

where x_p is the position of the first peak of the QM distribution, and the modulation is applied only for $0 \leq x \leq x_p$. Fig. 1 shows the results of this new model. It can be seen that the distribution obtained from this simplified method is in good agreement with the result of a full quantum-mechanical calculation with a large number of eigenstates in an extended quantum box, and for all bias conditions. The gate capacitance near flat bands for the *p*-MOS device of Fig. 1 is shown in Fig. 2. The discontinuity near flat bands is eliminated by the new model, without introducing any empirical parameter. Note also that a reduction in the gate capacitance due to QM effects can be seen even around flat bands, if the correct charge distribution is used. This method also ensures good convergence properties in all bias conditions, allowing an effective simulation of realistic device structures.

III. Gate Capacitance

Buried-channel n^+-poly/*p*-MOS devices with an oxide thickness of 8.7 nm and surface-channel transistors with oxide

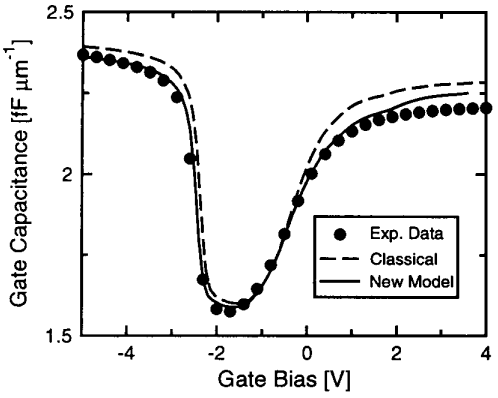

Fig. 5. Gate capacitance for surface-channel p-MOS device with peak channel doping of 1.1×10^{18} cm^{-3}.

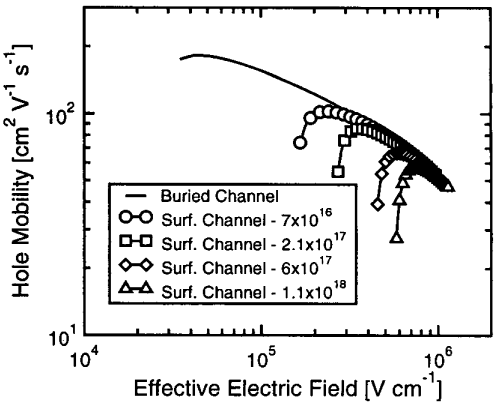

Fig. 6. Hole mobility as a function of the effective electric field, defined as $F_{eff} = (Q_{dep} + \eta Q_{inv})/\epsilon$, with $\eta = 1/3$.

thickness of 7.7 nm and channel doping between 7.3×10^{16} and 1.1×10^{18} cm^{-3} have been simulated. The metallurgical channel length is 0.35 μm and the width of the devices is 1.2 μm. Experimental data were obtained from arrays of 12 000 transistors, for a total gate area of 7.2×10^{-5} cm^2. Parasitic interconnect capacitances were estimated from 3D field simulations and subtracted from the results. Fig. 3 shows the comparison against experimental data for the gate capacitance of the buried-channel device. Figs. 4 and 5 show results for the surface-channel devices with the lowest and highest channel doping, respectively. Note that the 2D model correctly accounts for quantization in both the inversion and accumulation regimes, achieving a good agreement with the experimental data in all cases. The classical model, instead, significantly overestimates the gate capacitance in all bias conditions. The threshold voltage shift due to QM effects can also be observed in Fig. 5. We conclude that a detailed modeling of QM effects in all bias conditions is essential to obtain a reliable description of the gate capacitance in deep-submicron devices.

IV. Drain Current

The 2D model presented allows a detailed calculation of the impact of QM effects on the device drain current. To this aim, however, accurate models for the carrier mobilities are mandatory. Hole mobility data were extracted from buried- and surface-channel transistors, and are shown in Fig. 6 as a function of the effective electric field [14]. Note that the boron counterimplant in the buried channel device leads to a smaller transverse electric field over the whole operating region when compared to surface-channel transistors, hence to higher values of the hole mobility. The same universal behavior is however followed by all curves, indicating analogous scattering processes in the surface and buried channel devices.

A non-local mobility model has been developed, fitting the experimental data of Fig. 6. However, it is well known that the extracted value of the Coulomb mobility near the roll-off point

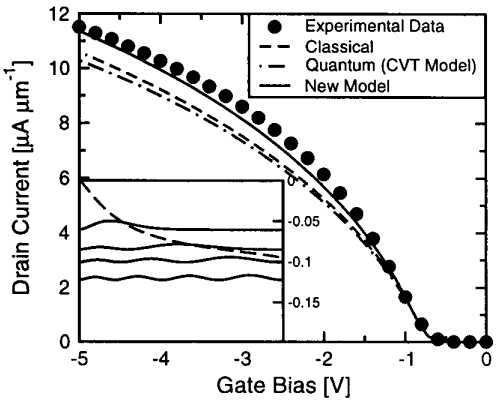

Fig. 7. Drain current at $V_D = -0.1$ V for a buried-channel device as computed from the different models. The inset shows the valence band at threshold up to 20 nm from the silicon/oxide interface (dashed line). The lowest four eigenvalues are also pictorially shown (solid lines).

is strongly affected by the diffusion current and by the existence of traps, making a reliable extraction very difficult. To avoid these uncertainties, we retained only the universal part of the mobility curve. The mobility, expressed as a function of the effective electric field, was calculated along each section and then interpolated without any significant overhead, in the same routine calculating the QM charge. However, from a physical standpoint, the extracted mobility should be ascribed to holes in the quantized well only, while carriers outside the quantum box and in the high-energy tail should retain their classical mobility. To this aim, the overall mobility was computed as an average between the above-mentioned nonlocal mobility and a conventional (CVT) mobility [15], weighed on the quantum and classical charge densities, respectively. Besides being physically reasonable, this solution eliminates any abrupt discontinuity in the carrier mobilities at the transition regions [8].

The drain current in the buried channel device computed at

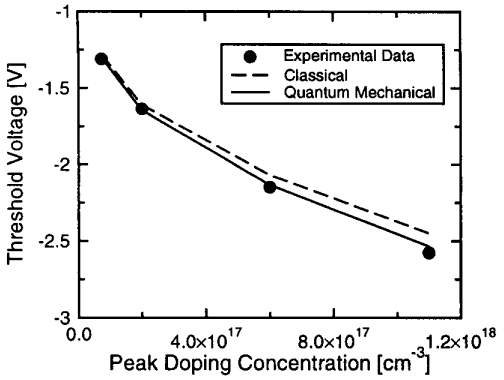

Fig. 8. Threshold voltages for surface-channel devices, as obtained from the classical and the new QM models.

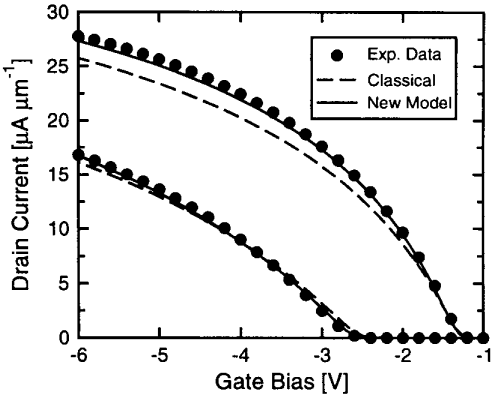

Fig. 9. Classical and QM drain currents for two surface-channel devices, compared with the experimental data.

$V_D = -0.1$ V is shown in Fig. 7. Note the negligible QM threshold voltage shift, due to the low surface electric field at threshold. The silicon valence band at threshold is shown in the inset of Fig. 7, up to a distance of 20 nm from the silicon/oxide interface. The resulting eigenvalues and eigenfunctions are also pictorially shown. Due to the boron counterimplant, the potential well is very weak and only a few levels are actually bound, determining a condition which is intermediate between the classical and the quantum regimes. As the gate bias is increased, the potential well narrows and QM effects appear, reducing the drain current below the classical value. Notwithstanding the low surface electric field, the CVT mobility model underestimate the drain current, which is instead reproduced correctly by the new model.

Fig. 8 shows the comparison against experimental data for the threshold voltages of the surface-channel devices. The classical estimate results in a maximum error of 100 mV over the whole doping range considered, which is reduced in the QM model to about 30 mV, considerably improving the match to experimental data.

Finally, the drain currents computed for the surface-channel devices with lowest and highest doping are reported in Fig. 9, for $V_D = -0.1$ V. It can be seen that the new model provides a better agreement with experimental data for all devices over the whole bias range.

V. Conclusions

We have developed a 2D MOS device simulator including QM effects. Convergence problems near flat bands have been avoided with a careful modeling of the charge distribution taking into account quantization effects at low vertical electric fields. To accurately describe the drain current in p-MOS devices, a nonlocal mobility model for holes has been developed and adopted. Results for the gate capacitance and the drain current are in good agreement with experimental data over a wide range of channel doping concentrations for both surface- and buried-channel devices.

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