Characteristics of Silicon Nano-Scale Devices

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Abstract—**Extremely small silicon MOS devices in a 10-nm scale are successfully fabricated and characterized at room temperature and low temperatures. In such small devices, quantum confinement effect and single electron charging effect manifest themselves in device characteristics even at room temperature. Device modeling challenges for nano-scale MOSFETs are also discussed.**

I. Introduction

The MOS devices in VLSI chips have been drastically scaled in these thirty years for higher performance and higher integration. The device size will become in the order of 10 nm in fifteen years when the scaling trend is simply extrapolated. It is well known that in such devices with extremely small dimension, the carriers are confined and quantum effects play an important role even in silicon devices. It has been observed that the direct tunneling current flows[1] when the gate oxide thickness is thin (less than 3 nm) and that the threshold voltage increases by surface quantization in the inversion layer in bulk MOSFETs with high impurity concentration[2]. Although these quantum effects have been well modeled, more quantum effects will take place if devices are smaller.

Besides the quantum effects that originate from the wave-like nature of electrons, the number of electrons in a device significantly decreases as the device shrinks, resulting in the single electron charging effect[3]. When the devices size is less than 10 nm, the Coulomb blockade is clearly observed even at room temperature [4], [5], [6]. Therefore, both quantum effect and single electron effect should be precisely modeled in 10-nm scale devices for future VLSI chips.

In this study, extremely small MOSFETs in less than 10 nm are successfully fabricated using VLSI-compatible process and their characteristics are extensively investigated at room temperature and low temperatures. It is found that in devices with extremely narrow channel, the quantum confinement effect is enhanced by lateral confinement that leads to large threshold voltage increase at room temperature [7], [8]. When these devices are cooled down, the single electron charging effect also becomes dominant. It is shown that device characteristics are largely distributed by slight potential fluctuations in the small channels even if the geometrical size is the same. Device modeling challenges for nano-scale MOSFETs are also discussed.

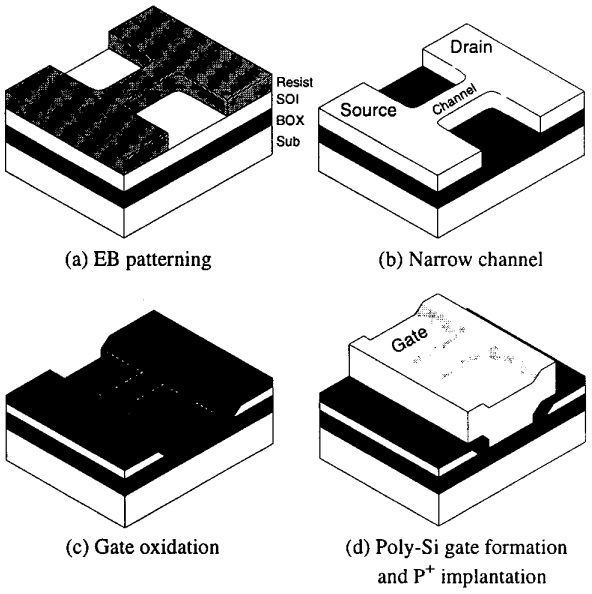

Fig. 1. Fabrication steps of ultra-narrow channel MOSFETs on a (100) SOI wafer. (a) A narrow channel pattern is formed by EB lithography. (b) The pattern is transferred to very thin SOI layer by RIE. (c) Gate oxidation is performed (34 nm). (d) A normal process is used for MOSFET fabrication. The final SOI thickness is 7 nm.

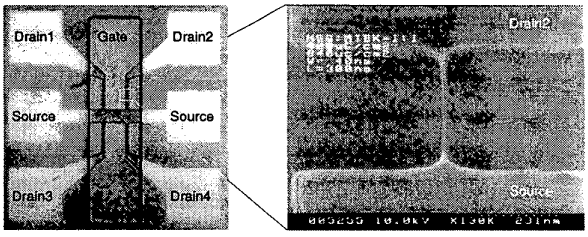

Fig. 2. Top views of fabricated ultra-narrow channel MOSFETs. (a) The whole test pattern with four devices. (b) SEM image of a narrow channel. The channel width is 10 nm.

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II. Extremely Narrow Channel MOSFETs

A. Fabrication

Nano-scale MOSFETs with extremely narrow channels are fabricated on an extremely thin silicon-on-insulator (SOI) wafer by electron-beam (EB) lithography and reactive ion etching (RIE). Fig. 1 shows the fabrication steps of the ultra-narrow channel MOSFET. The channel is oriented along the (110) direction. The final thickness of SOI layer is 7 nm. Fig. 2 shows the top views of fabricated MOSFETs. A scanning-electron-microscope (SEM) image is shown in Fig. 2 (b). The channel width is 10 nm in this particular device. The channel is not fluctuated along the channel. In order to investigate the width dependence of device characteristics, the channel widths are widely varied from almost 0 nm to 45 nm. The standard deviation of the channel width distribution is less than 2 nm.

B. Room temperature characteristics

Figures 3 and 4 show the gate voltage dependence of drain current in a linear scale and in a logarithmic scale, respectively, at room temperature. Good subthreshold swing (S $\sim$ 100 mV/dec) is obtained even though the width is 10-nm scale. Drain current is not proportional to channel width because the source and drain resistance is quite high due to thin SOI layer. Fig. 5 shows the channel width dependence of threshold voltage. Threshold voltage increases as the channel becomes narrower, particularly below 10 nm.

C. Calculation of threshold voltage shift

To investigate the origin of the threshold voltage increase in narrow channel MOSFETs, energy states in conduction band are calculated solving the two-dimensional steady state Schrödinger equation with effective mass approximation by the finite element method[7], [8]. Anisotropic effective mass of electrons in silicon and electron penetration into SiO_2 are taken into account. The threshold voltage shift is derived from the lowest state energy. Fig. 5 also shows the calculation results. The experimental data and calculation results are in good agreement, indicating that the threshold voltage increase is caused by the quantum confinement.

The threshold voltage increase has been also observed in extremely thin SOI MOSFETs with relatively wide channel[9] when the SOI thickness is less than 6 nm. Since the channel is not only thin but also narrow in our devices, the device size at which the threshold voltage increases (10 nm) is larger. The enhancement of threshold voltage increase in narrow and thin channel MOSFET is also confirmed by the calculation[7], [8]. These results indicate that more quantum confinement effects are expected when the device shrinks in both lateral and depth directions.

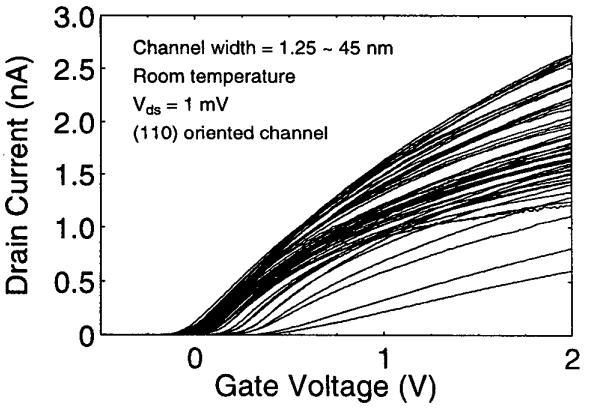

Fig. 3. I_{ds}-V_{gs} characteristics of the fabricated ultra-narrow MOSFETs in a linear scale at room temperature.

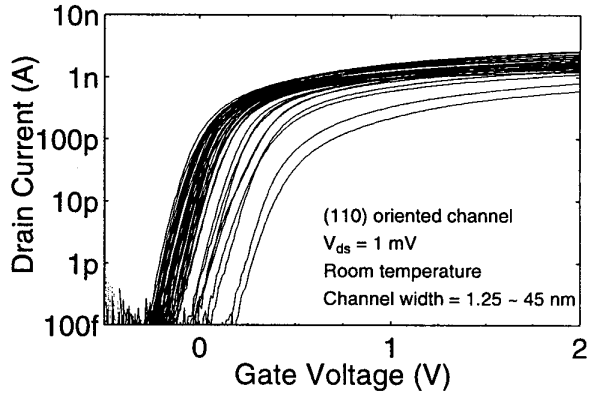

Fig. 4. I_{ds}-V_{gs} characteristics of the fabricated ultra-narrow MOSFETs in a logarithmic scale at room temperature.

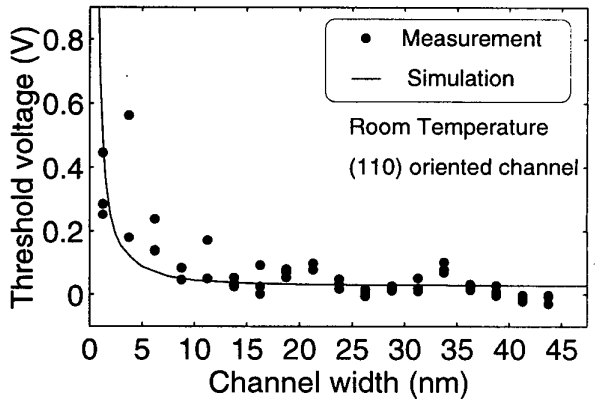

Fig. 5. Channel width dependence of threshold voltage. The experimental data and calculation results are compared. They are in good agreement, indicating that threshold voltage shift in narrow channel is caused by the quantum confinement effect.

D. Low temperature characteristics

Figure 6 shows the low temperature characteristics of ultra-narrow MOSFETs whose room temperature characteristics are shown in Figs. 3 and 4. When the temperature decreases, aperiodic random oscillations are observed in I_{ds}-V_{gs} characteristics. The oscillations are enhanced as the temperature decreases and the channel width decreases. This phenomenon is called as Coulomb blockade caused by the single electron charging effect in a multiple dot system [5]. Due to the channel width fluctuations and discrete fixed charges, the potential in the channel is fluctuated that leads to several potential barriers and islands in the channel[10]. These results suggest that not only quantum confinement effect but also single electron charging effect is dominant in transport in extremely small devices.

III. Extremely Narrow and Short Channel MOSFET

Devices in the previous section have very narrow channel but the channel length is relatively long. Then, the characteristics are averaged along the channel. In this section, characteristics of devices with narrow and short channel are shown, where averaging effect is negligible and the characteristics vary depending on samples even when the geometrical shape and size is the same.

A. Characteristic distribution

Figure 7 shows schematics of a point-contact MOSFET that has an extremely constricted channel. Since the length of the constricted region is very small, the number of potential islands is expected to be one or two. Fig. 8 shows room temperature I_{ds}-V_{gs} characteristics of point-contact MOSFETs that are fabricated in a very uniform manner by anisotropic etching technique[11]. The width of the point-contact channel is less than 30 nm. The drain current distribution is less than ±10%, which is small enough considering the width is extremely narrow.

At low temperature, however, the characteristics are very different as shown in Fig. 9. Some devices show normal characteristics, while some devices show small or large Coulomb blockade oscillations. When the number of potential island dots is one, the oscillations are periodic as shown in the figure. The large characteristic distribution at low temperature is caused by the slight potential distribution in small channel even when the geometrical shape and size are the same.

B. Large Coulomb blockade at room temperature

Figure 10 shows the I_{ds}-V_{gs} curve at room temperature in a device with an extremely small dot (less than 5 nm). Large Coulomb blockade oscillations can be observed when the dot size is extremely small. When the dot size is in a 5-

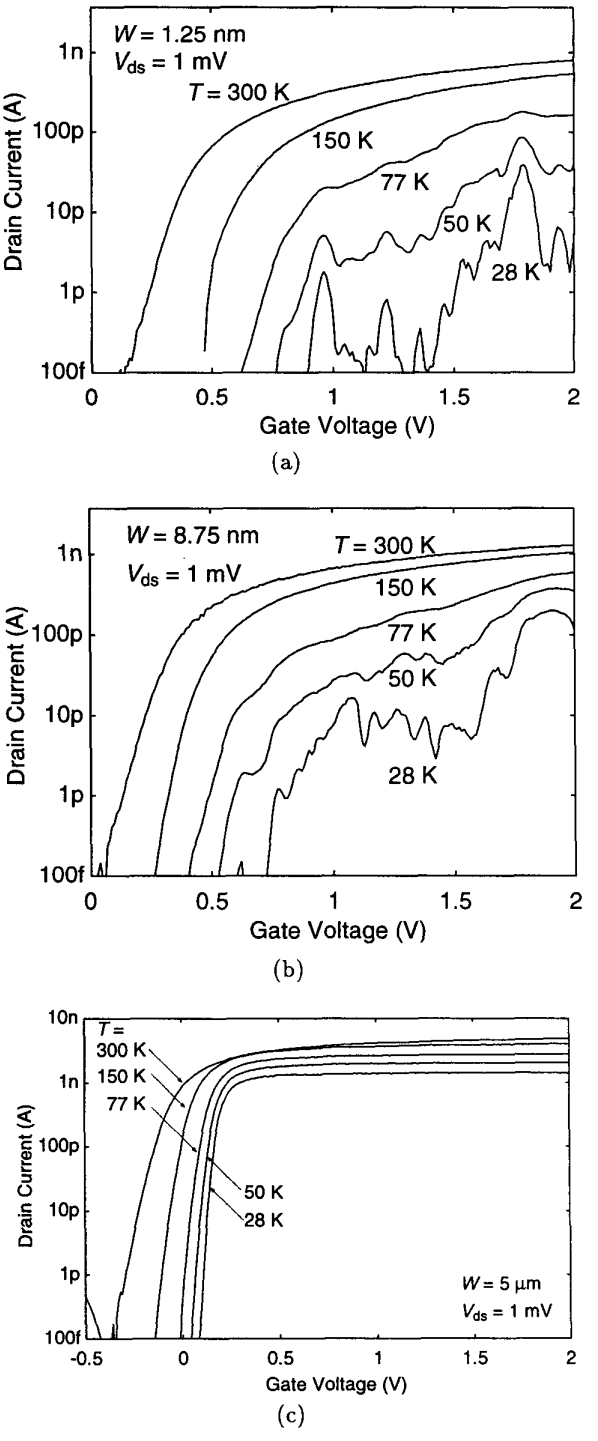

Fig. 6. I_{ds}-V_{gs} characteristics of ultra-narrow MOSFETs at low temperatures. The devices are the same as those shown in Figs. 3 and 4. (a) $W = 1.25$ nm. (b) $W = 8.75$ nm. (c) Reference device with $W = 5$ μm.

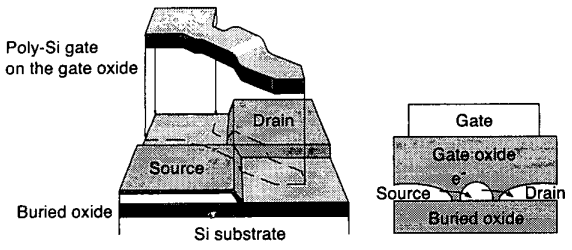

Fig. 7. A schematic bird-eye view and a cross section of a point-contact MOSFET. The channel is extremely constricted at one point.

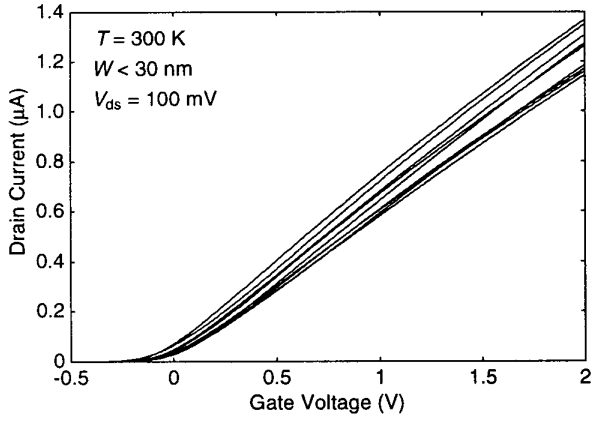

Fig. 8. I_{ds}-V_{gs} characteristics of point-contact MOSFETs at room temperature. The distribution of drain current is less than ± 10%.

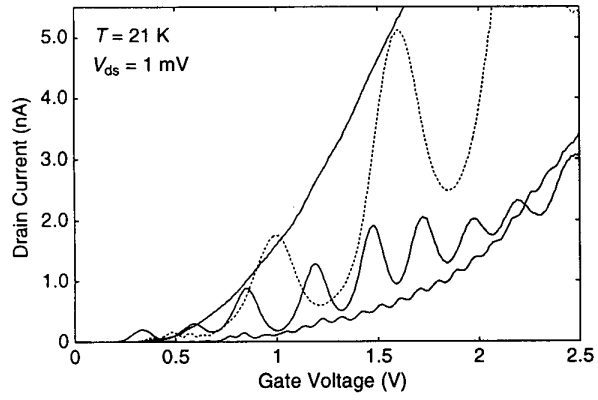

Fig. 9. I_{ds}-V_{gs} characteristics of point-contact MOSFETs at 21 K. The devices are the same as those shown in Fig. 8. The characteristics largely distribute.

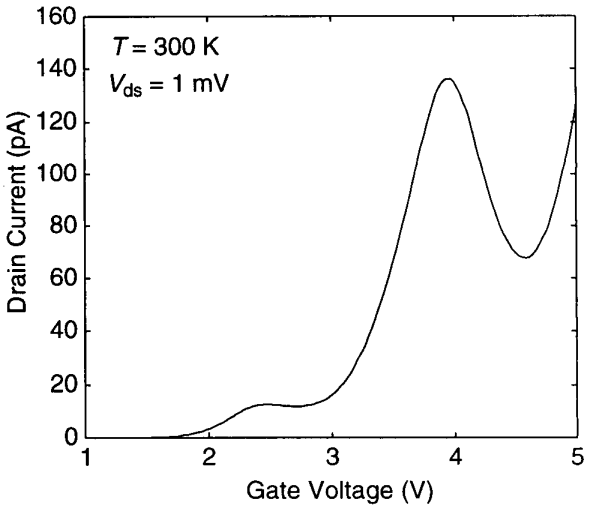

Fig. 10. Characteristics of a point-contact MOSFET with an extremely small dot (less than 5 nm) at room temperature. Large Coulomb blockade oscillations are observed.

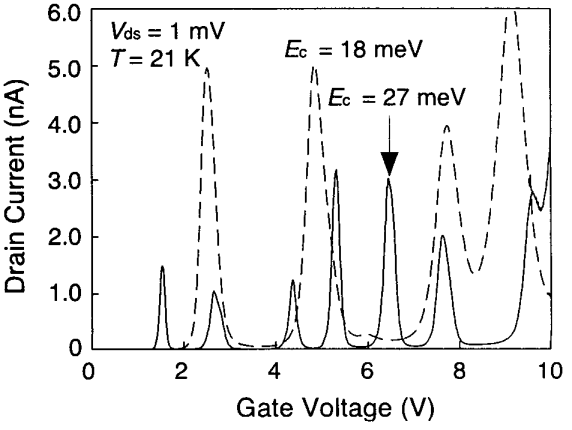

Fig. 11. Aperiodic Coulomb blockade oscillations in point-contact MOSFETs with dots smaller than 10 nm. Derived charging energy (E_c) is shown.

nm scale, the electron energy states in the dot are separated and the Coulomb blockade oscillations become aperiodic [6], as shown in Fig. 11. These results indicate that even at room temperature the slight potential fluctuations affect characteristics of nano-scale devices and that the large characteristics distribution observed in Fig.10 could also be observed at room temperature.

IV. Device Modeling Challenges

All the experimental data shown above indicate that quantum confinement effect and single electron charging effect should be precisely included in the simulation for the future nano-scale MOSFETs. When the geometrical device

shape and size are given, the quantum states, tunneling rates, and master equations can be solved and the device characteristics can be basically calculated. However, one of the most difficult issues is to derive the potentials within a device that is easily affected by random distribution of fixed charges, interface states, and dopant atoms.

It is well known that threshold voltage fluctuations are caused by the statistical distribution of impurity atoms[12], [13]. In nano-scale devices, the statistical fluctuations are largely enhanced because the quantum effect and single electron charging effect are very sensitive to slight potential distribution. The main challenges for future device modeling are not only the incorporation of quantum and single electron effects, but also the exact modeling and incorporation of statistical nature of atoms and electrons.

V. Conclusion

Extremely small silicon MOS devices in a 10-nm scale are successfully fabricated and characterized at room temperature and low temperatures. In such small devices, quantum confinement effect and single electron charging effect play important roles in device characteristics even at room temperature. The incorporation of statistical nature of atoms would be the main challenges for device modeling of nano-scale MOSFETs.

Acknowledgments

The authors would like to thank N. Takahashi and M. Saitoh for device measurements and discussion. This work was in part supported by the Grant-in-Aid of Scientific Research from the Ministry of Education, Science, Sports, and Culture, Japan.

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