Two-Dimensional Bandgap Engineering in a Novel Si/SiGe pMOSFET With Enhanced Device Performance and Scalability

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Abstract – Two-dimensional device simulations are used to explore the applications of bandgap engineering in improving device performance and scalability. Heterojunction pMOSFETs with strained SiGe in the source and/or drain have substantially suppressed short-channel effects, including field-induced barrier lowering in the devices with high-K gate dielectrics/spacers. Despite the source-side velocity overshoot, the drive currents in these devices are reduced due to the hetero-barriers in the channel. This drawback can be eliminated by the use of a thin Si or SiGe cap layer. Finally, a novel pMOSFET with a SiGe source/drain and a SiGe quantum well channel is proposed. It has reduced SCE and enhanced drive current.

I. Introduction

Silicon MOSFET scaling has become a major challenge in the semiconductor industry. Traditional techniques start to fail in reducing certain undesirable physical effects as device dimensions shrink down to the nanometer regime [1-2]. With bandgap engineering a very important degree of freedom can be provided in device design. Recently, higher hole mobility in strained SiGe [3] has been demonstrated, and very high speed has been achieved in p-type strained SiGe or Ge channel MODFETs [4-5]. On the other hand, the valence band offset in a heterojunction pMOSFET (HJMOSFET) with a strained-SiGe source/drain (S/D) has been found to be very effective in reducing short-channel effects (SCE) such as drain-induced barrier lowering (DIBL) and bulk punchthrough [6-9]. The drawback of such devices is much lowered drive current due to reduced "source injection" [10]. In this study, two-dimensional device simulations are used to further explore new device structures for improving performance and scalability, and a novel pMOSFET with reduced SCE and enhanced drive current is proposed.

II. Device Concepts and Simulation Method

Three types of device structures have been studied. In device A, compressively strained SiGe is used in the S/D (Fig. 1); in device B, a thin Si cap or strained-SiGe cap is added to device A (Fig. 2); in device C, a Si/SiGe/Si quantum well channel is added to device A (Fig. 3). The devices with 100 nm gate length and 2.5 nm gate oxide thickness are simulated using MINIMOS-NT [11]. Unlike the previous studies [6-7], in which a post-processing tunneling model was used to estimate the drive current, self-consistent solutions of thermionic-field emission [12] and drift-diffusion are obtained in this study, and quantum mechanical tunneling is taken into account through field-induced barrier lowering.

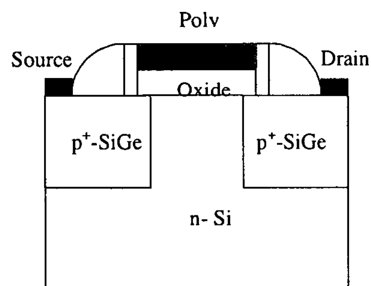

Fig. 1. Schematic of a symmetric HJMOSFET with strained SiGe in the S/D (device A).

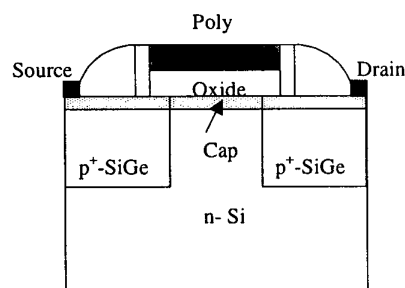

Fig. 2. Schematic of an HJMOSFET with a thin layer of Si or SiGe cap (device B).

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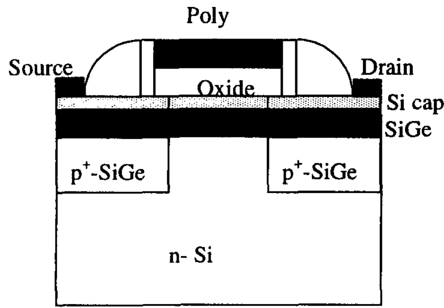

Fig. 3. Schematic of a novel pMOSFET — a high mobility heterojunction transistor (device C).

III. Results and Analysis

Reduced bulk punchthrough and DIBL have been achieved in vertical pMOSFETs with strained SiGe in the source [8-9], similar to device A. This is because the hetero-barriers provided by the band offset are not lowered by high drain biases, which can be seen in Fig. 4. Furthermore, fringing field induced barrier lowering (FIBL) that increases the off state leakage current (I_{off}) in the device with high-K gate dielectric and spacers [13-14], is also reduced if strained SiGe is used in the S/D, as shown in Fig. 5. The drawback of HJMOSFETs is degraded drive current (I_{on}) due to the hetero-barriers in the channel (shown in Fig. 4).

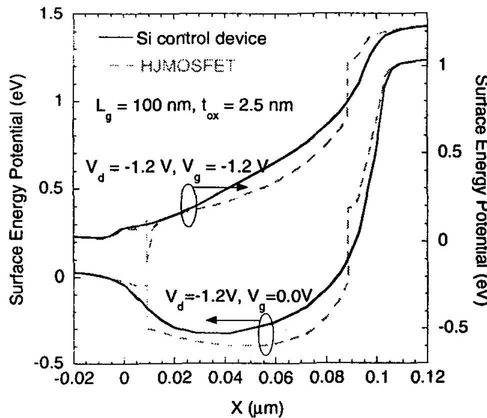

Fig. 4. Surface energy potentials of an HJMOSFET with a $Si_{0.6}Ge_{0.4}$ S/D and a control Si device in the "on" state and the "off" state.

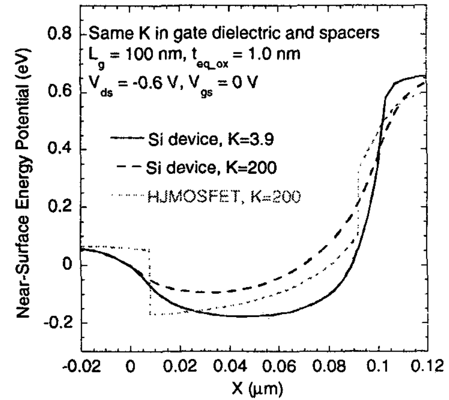

Fig. 5. Energy potentials at 1 nm below the surface in the "off" state of a control Si device with oxide in the gate dielectric and spacers, its counterpart Si high-K device, and a $Si_{0.6}Ge_{0.4}$ HJMOSFET with a high-K material in the gate dielectric/spacers.

Although source-side velocity overshoot may occur after the carriers pass the hetero-barrier due to the large band bending caused by high gate voltages (Fig. 6), the carrier transport is mainly governed by the quantum mechanical tunneling through the hetero-barrier, and the carrier concentration is lower compared to a Si control device.

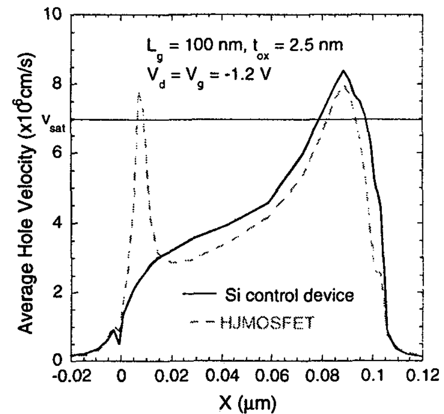

Fig. 6. Average velocity (over the carrier concentration) in a $Si_{0.6}Ge_{0.4}$ HJMOSFET and a control Si device. The results are obtained from Monte Carlo simulations using UTMC2D [15].

The drive current in HJMOSFETs can be significantly enhanced by the use of a thin Si or SiGe cap layer (device B). The absence of the hetero-barriers in the cap layer improves the drive current substantially without sacrificing the off-state leakage caused by DIBL and bulk punchthrough. Compared to the HJMOSFET with no cap layer, the drive current is increased by 52% in the device with a 5 nm Si cap layer and 364% in the one with a 5 nm $Si_{0.6}Ge_{0.4}$ cap layer. It should be mentioned that the expected higher SiGe/oxide interface state densities are not accounted for in the simulations. In the case of the Si cap, the improvement is entirely due to the enhanced source injection. In the case of the SiGe cap, 56% of the total improvement (364%) is due to higher hole mobility in SiGe, 30% is due to a smaller flat band voltage in SiGe, and 14% is due to the enhanced source injection. As the cap thickness increases, the enhancement in the drive current tends to saturate, and the leakage current starts to increase (Fig. 7). The maximum I_{on}/I_{off} ratio is achieved at a cap layer of 5-10 nm, which is about the same thickness as the inversion layer in these devices.

Process concerns suggest that a thin layer of Si be used as a sacrificial layer for gate oxidation to achieve a high-quality interface [8]. Therefore, we propose a novel pMOSFET (device C) with a SiGe S/D and a Si/SiGe/Si quantum well channel, where bandgap engineering is performed in a two-dimensional fashion (along the channel and perpendicular to it). We call such a device a high mobility heterojunction transistor (HMHJT). For 1.5 V applications, the I_{on}/I_{off} ratio in an HMHJT with a 1 nm Si cap, a 5 nm $Si_{0.6}Ge_{0.4}$ channel, and no anti-punchthrough implant is 6×10^7, which is 180X higher than that of a conventional 100 nm Si pMOSFET with a similar linear threshold voltage (~-0.4 V) fabricated by Rodder *et al.* [16]. For 1.2 V applications, compared to an *optimized* conventional 100 nm Si device [17], an HMHJT with the same doping profile and a p^+-poly SiGe gate has the same off state leakage and a 2X higher drive current. It may be noted that the reduced poly depletion and boron penetration in the p^+-poly SiGe gate [18] are not included in this study; otherwise, the expected enhancement should be even greater. The I_d-V_g characteristics are shown in Fig. 8. As the two technologies scale, reduced SCE are predicted in the HMHJTs. The comparisons of the subthreshold swing and V_T roll-off are shown in Fig. 9, and the I_{off}-I_{on} characteristics are illustrated in Fig. 10.

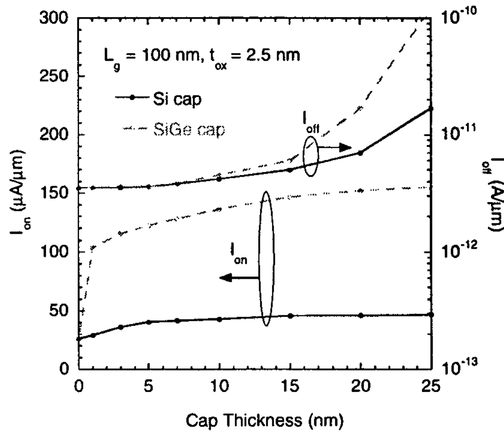

Fig. 7. I_{on} ($V_{ds} = V_{gs}$ = -1.2 V) and I_{off} (V_{ds} = -1.2 V, V_{gs} = 0 V) versus the thickness of the Si or $Si_{0.6}Ge_{0.4}$ cap layer for a fixed channel doping.

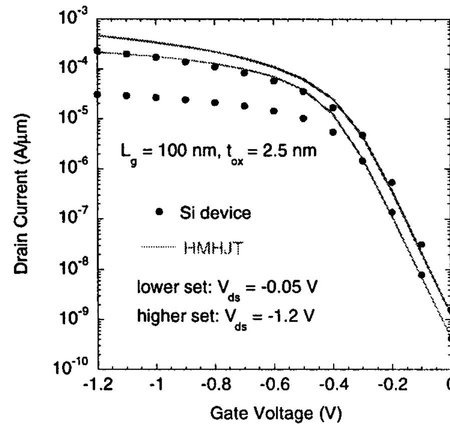

Fig. 8. I_d-V_g characteristics at V_{ds} = -0.05 V and –1.2 V for the optimized 100 nm Si device and a $Si_{0.6}Ge_{0.4}$ HMHJT.

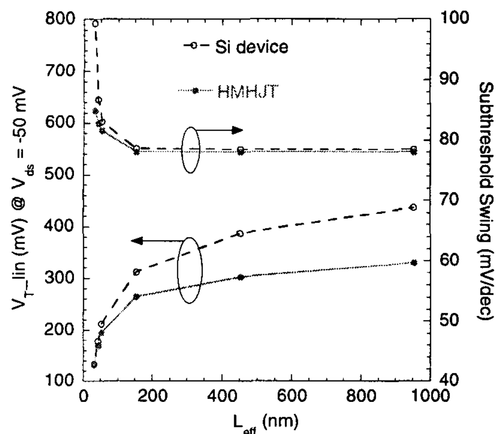

Fig. 9. Subthreshold swing and V_T roll-off versus metallurgical channel length (L_{eff}) for the devices of Fig. 8.

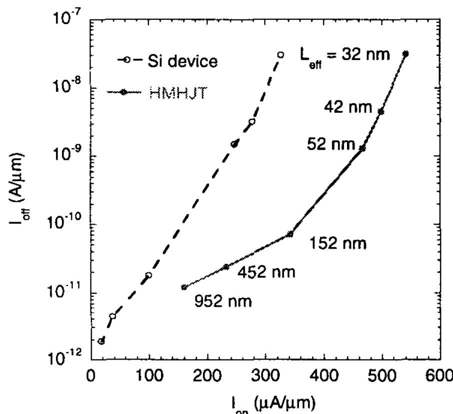

Fig. 10. I_{off} (V_{ds} = -1.2 V, V_{gs} = 0 V) versus I_{on} (V_{ds} = V_{gs} = -1.2 V) for the devices of Fig. 8.

The fabrication of the novel HMHJT device is expected to be similar to that of SiGe channel MOSFETs. The Si cap layer and SiGe channel layer can be grown by CVD, and the deep SiGe source/drain can be formed by high-energy Ge implantation or selective epitaxial growth.

IV. Conclusions

The band offsets in the HJMOSFETs with a strained SiGe S/D are very effective in reducing SCE. The drawback of lowered drive current in HJMOSFETs can be overcome by using a thin Si or SiGe cap layer. The optimal cap layer thickness is found to be similar to that of the inversion layer. Moreover, a novel pMOSFET with a SiGe S/D and a SiGe quantum well channel is proposed. Improved device performance and scalability are predicted in this new device structure.

V. Acknowledgement

The authors would like to thank Dr. Siegfried Selberherr for the use of MINIMOS-NT. Special thanks go to Dr. Hans Kosina, Dr. Tibor Grasser and Dr. Claus Fischer for technical support and insightful discussions.

This work was supported in part by the Semiconductor Research Corporation, the DoD-MURI program, and NSF-STC.

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