DC and AC Performance Analysis of 25 *nm* Symmetric/Asymmetric Double-Gate, Back-Gate and Bulk CMOS

MeiKei Ieong, H-S Philip Wong*, Yuan Taur* , Phil Oldiges, and David Frank*

IBM SRDC, Z/AE1, 2070 Route 52, Hopewell Junction, NY 12533

*IBM T.J. Watson Research Center, Yorktown Heights, NY 10598, USA

E-mail: mkieong@us.ibm.com Phone: (914) 892-4719 Fax: (914) 892-3039

Abstract- **In this paper, the performance of 25 nm double-gate, back-gate and super-halo CMOS devices has been analyzed including self-consistent 2D quantization effect. The drive current is enhanced by gate-to-body coupling effect for double-gate with ultra-thin body. The channel quantization effect can substantially degrade the drive-current for asymmetric double-gate, back-gate, and bulk CMOSs. It is demonstrated that the exceptional SCE immunity in SDG offers substantial performance leverage over conventional MOSFET structures.**

I. INTRODUCTION

Double-gate and back-gate MOSFETs with ultrathin body are considered the most promising candidate for CMOS scaled to the ultimate limit of 15-30 nm gate lengths [1-4]. Earlier device design analyses [2,5] had already identified the basic design criteria such as a thin (5-10 nm) silicon channel, self-aligned top and bottom gates, and a source/drain fan-out. Experimental demonstration of MOSFETs bearing such characteristics are actively being pursued [1,6-8] at several laboratories. In this paper, we extend the performance analysis of double-gate and back-gate MOSFET's to include the effects of 2-D quantization in the very thin (< 10 nm) silicon channel in the sub-threshold and above-threshold analyses, and to compare the circuit delay among different device architectures.

II. QUANTUM EFFECT ON DOUBLE-GATE MOSFET

For the first time, device and circuit performance of double-gate and conventional MOSFETs including complete quantization effect are evaluated through self-consistent solution of Schrodinger, Poisson, Continuity, and external circuit equations. The quantized carrier is obtained by solving the 1-D Schrodinger equation along the 2-D MOSFET channel. This quantum charge is iteratively coupled with the drift-diffusion equation used in *Fielday* [10] through an efficient algorithm described in [9]. With this 2-D quantum model, the 2-D charge density can be accurately predicted. In the absence of an efficient, reliable, and more accurate carrier transport model, we used the drift-diffusion equations with mobility parameters calibrated to 50nm gate-length experimental SOI CMOS data [15]. The predicted saturated current provides relative performance comparison among various device structures.

A generic double-gate MOSFET structure is shown in Fig.1. The threshold voltage of a double-gate MOSFET with poly-silicon gate only is not suitable for normal operation.

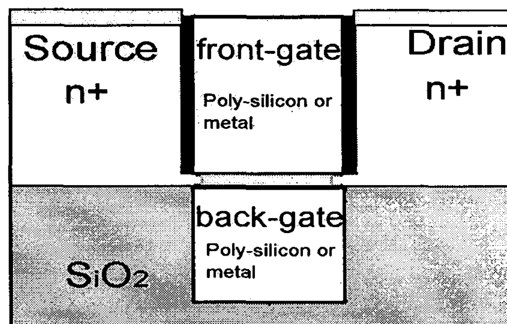

Fig.1 : Generic double-gate MOSFET : A) symmetric double-gate (SDG) with gate workfunction of 250mV above mid-gap for both front- and back-gate ; B) asymmetric double-gate (ADG2) with n+ for front-gate and 200 mV below mid-gap for back-gate; C) asymmetric double-gate (ADGP) with n+ for front-gate and p+ for back-gate; D) back-gate MOSFET (BG) with n+ for front-gate and mid-gap for back-gate.

To adjust the threshold voltage, different gate materials can be used, thereby allowing the gate workfunction to be tuned. Some possible combination of gate workfunctions suitable for normal MOSFET operations are listed in Fig.1. Note that both the front- and back-gate are tied together for SDG and ADG operation. The back-gate is tied to a fixed bias for BG operation. Fig.2 displays the potential energy at the off condition.

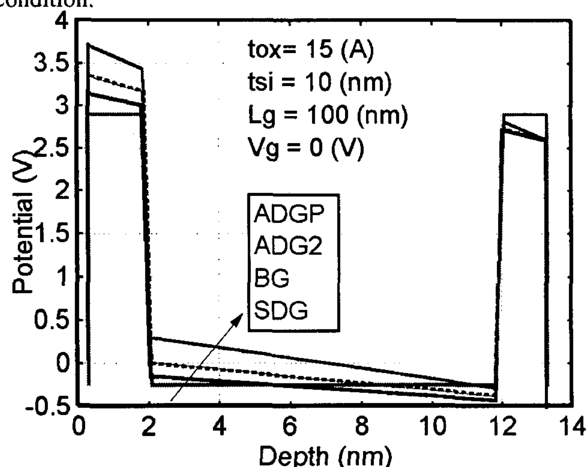

Fig.2 : Potential energy for SDG, BG, ADG2, and ADGP MOSFETS. The channel is undoped.

0-7803-6279-9/00/$10.00 © 2000 IEEE

It can be seen that different choices of gate workfunction materials give rise to symmetric and asymmetric band-diagrams. The quantum induced Vt shift in SDG can be substantially reduced due to a relatively flat and symmetric energy band-diagram [11].

III. POTENTIAL ENERGY SYMMETRY EFFECT

The electron charge distribution vs. silicon film thickness at common gate overdrive (Vg-Vt) for SDG and BG is shown in Fig.3. The SDG exhibits a more uniform inversion charge density as the silicon film thickness is scaled down. However, quantization effect dominates the BG MOSFET. The integrated charge for the BG MOSFET is indeed decreased for thinner silicon films [11]. It is obvious that the quantization effect must be considered for double-gate MOSFET design tradeoffs.

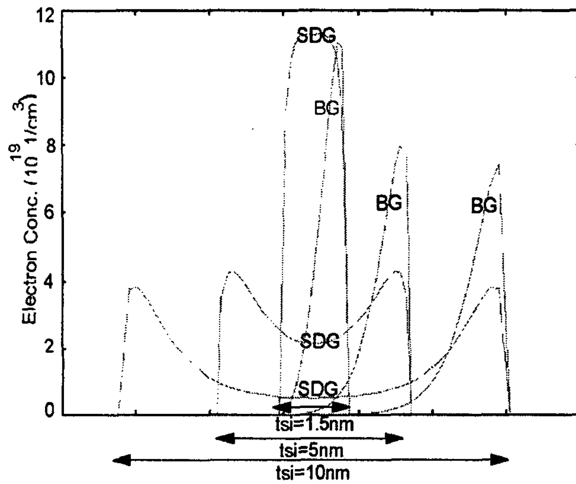

Fig.3. : Electron concentration distribution perpendicular to the oxide interface for SDG and BG at Vg= Vt + 0.8 V.

As the silicon film thickness decreases, the gate field effectively reduces the drain-induced barrier lowering (DIBL) and short-channel effect (SCE) by shielding the source/drain field. As the silicon film becomes thinner in the SDG case, the threshold leakage current decreases for a given potential. This improves the Ion-Ioff characteristics of SDG. As shown in Fig. 4, BG operation has the worst SCE and DIBL, as expected. Under double-gate operations, the short-channel characteristic is affected by the degree of symmetry of the gate workfunction. The SDG has the smallest Vtsat rolloff while the n+/p+ gate ADGP has the largest (SCE). It is interesting that the ADGP exhibits a better DIBL (see Fig.5).

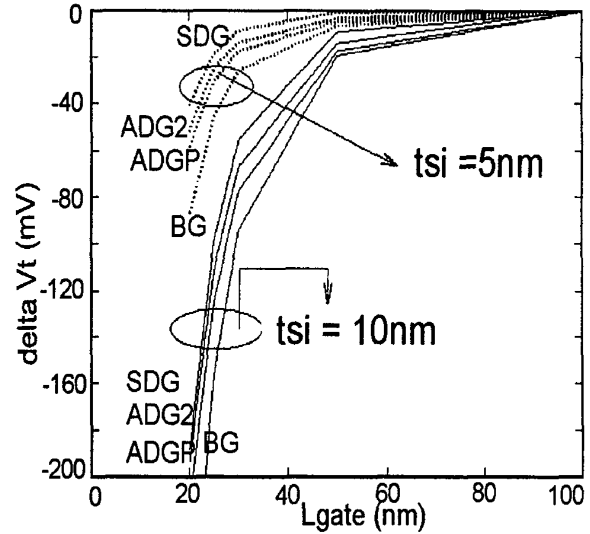

Fig.4 : Vt rolloff curves for BG and DG with different gate workfunction configurations.

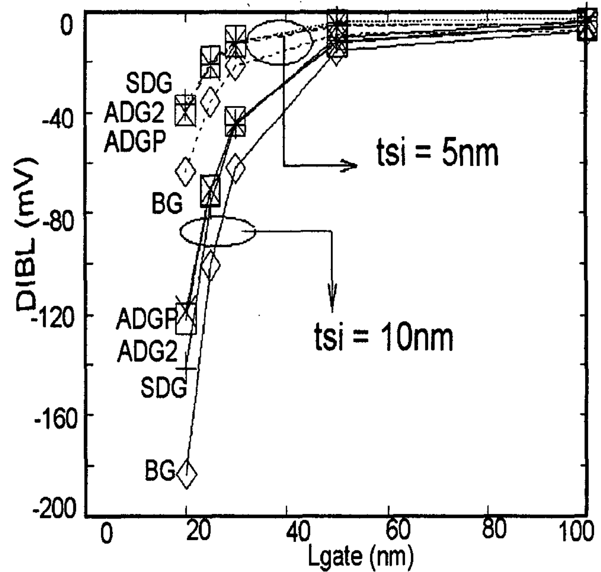

Fig.5 DIBL for BG and DG with different gate workfunction configurations.

IV. PERFORMANCE COMPARISON

The Ion-Ioff characteristic for BG and DG with different gate workfunction configuration is shown in Fig.6. The SDG with tsi=5nm gives the best Ion-Ioff tradeoff. A four time reduction of the S/D doping concentration can degrade the drive-current by about ten percent. Therefore process technique that provides low contact resistance and high active doping concentration are crucial. From our simulations, the halo (or channel-length dependent channel doping) design in such thin-body double-gate MOSFET does not provide any advantage. In fact, the drive-current can be severely degraded due to mobility degradation.

The Id-Vgs characteristics of 25nm SDG, ADG and Super-halo [12] CMOS devices are compared in Fig.7. The channel doping has been adjusted to give the same off current for all three devices. The SDG has higher Idsat, compared to that of ADG and 2X of Bulk CMOS, due to more effective charge coupling and higher mobility with its lower fields. The bulk CMOS current is about 10-15% lower than ADG and SDG due to lower gate over-drive originated from a worse subthreshold swing. The inverter delay for the three device architectures has also been evaluated by mixed-mode simulation including the full quantization effect. For a constant capacitor loading (6fF), 14% and 18% performance gains over bulk CMOS can be achieved by ADG and SDG, respectively. In Fig.8, the CV/I metric is used to benchmark the simulated intrinsic device performance with previously published experimental bulk and SOI data. At an Ioff of 10 *nA/um*, the CV/I metric for SDG is 0.72 ps at 1.0V. This clearly demonstrates the advantage of SCE control in double-gate MOSFET.

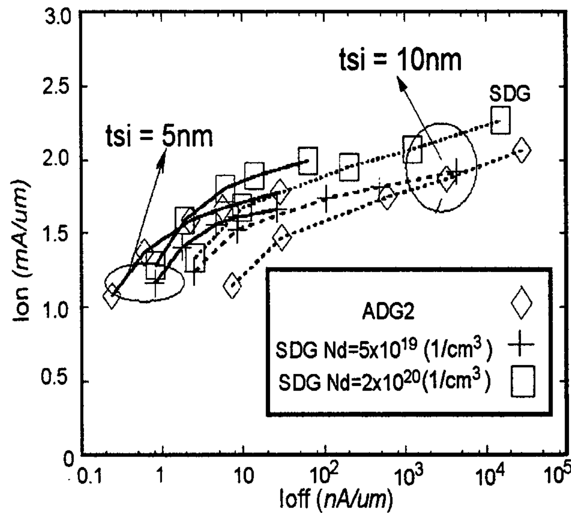

Fig.6 : Ion-Ioff characteristics for different gate workfunction configurations and S/D doping concentration. (solid line : tsi=5nm; dotted line : tsi=10nm)

V. CONCLUSIONS

In this paper, the performance of 25 nm double-gate, back-gate and super-halo CMOS devices has been analyzed including self-consistent 2D quantization effect. The drive current is enhanced by gate-to-body coupling effect for double-gate with ultra-thin body. The channel quantization effect can substantially degrade the drive-current for asymmetric double-gate, back-gate, and bulk CMOSs. It is demonstrated that the exceptional SCE immunity in SDG offers substantial performance leverage over conventional MOSFET structures.

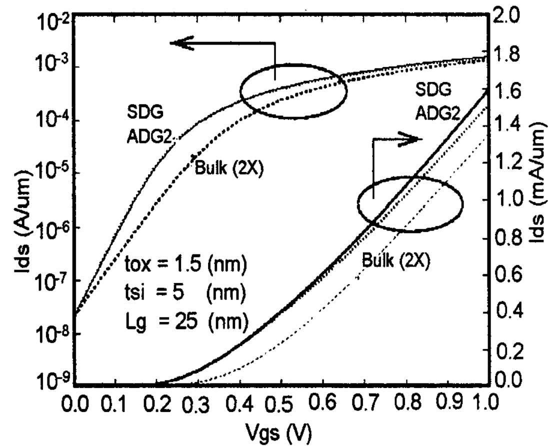

Fig.7 : Ids-Vgs characteristics of the SDG, ADG, and Super-halo bulk NMOS (The drain current of the bulk MOSFET is scaled by two to compare with the two gates in the double-gate devices). Channel doping is adjusted to the same Ioff.

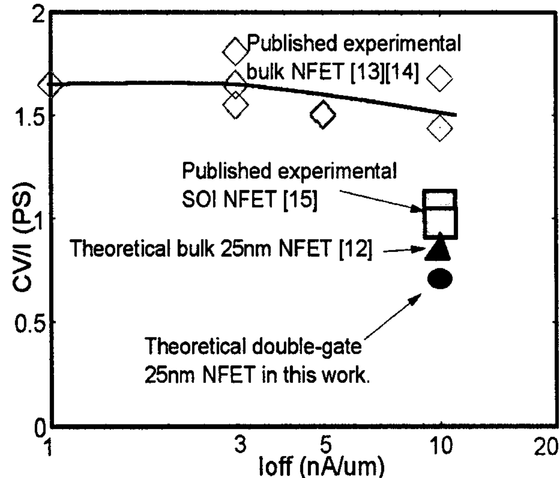

Fig.8 : CV/I metric vs. Ioff for simulated and published experimental data. The published experimental NFET has longer channel length.

ACKNOWLEDGMENT

The authors would like to acknowledge Steve Laux, Max Fischetti for useful discussions. Management support from Dr. John Warlaumont is very much appreciated.

REFERENCES

[1] X. Huang *et al.*,"Sub 50-nm FinFET:PMOS", *IEDM Technical Digest,* pp.67-70, 1999.

[2] H.-S. P. Wong, D. J. Frank, and P. M. Solomon, "Device Design Consideration for Double-Gate, Ground-Plane, and Single-Gated Ultra-Thin SOI MOSFET's at 25nm Channel Length Generation," *IEDM Technical Digest*, pp.407-410, 1998.

[3] C. Fiegna, H. Iwai, T. Wada, T. Saito, E. Sangiorgi, and B. Ricco, "A new scaling Methodology for the 0.1-0.025 μm MOSFET," in *Symp. VLSI Technology Technical Digest,* pp.33-34, 1993.

[4] D. J. Frank, S. E. Laux, and M. V. Fischetti, "Monte Carlo Simulation of a 30nm dual-gate MOSFET: How short can Silicon go?," *IEDM Technical Digest,* pp.553-556, 1992.

[5] H.-S. Wong, D. Frank, Y. Taur, and J. Stork, "Design and performance considerations for sub-0.1-μm double-gate SOI MOSFET's," *IEDM Technical Digest,* pp.747-750, 1994.

[6] H-S. Wong *et al.,* "Self-Aligned (Top and Bottom) Double-Gate MOSFET with a 25 nm Thick Silicon Channel," *IEDM Technical Digest,* pp.427-430, 1997.

[7] D. Hisamoto *et al.,* "A Folded-channel MOSFET for Deep-sub-tenth Micro Era," *IEDM Technical Digest* , pp.1032-1034, 1998.

[8] H.-S. Wong *et al.,IEEE Proc.*,p.537,1999.

[9] M. Ieong *et al.*, *"3rd NASA Workshop on Device Modeling",* 1999.

[10]E.M. Buturla, P.E. Cottrell, B.M. Grossman, and K.A. Salsburg, "Finte-element analysis of semiconductor devices: the FIELDAY program," *IBM J. Res. Develop.,* vol. 25, p. 218, 1981.

[11] M. Ieong *et al., submitted to IEEE EDL.*

[12] Y. Taur *et al.,* '25 nm CMOS Design Considerations," *IEDM Technical Digest*, p.789-792, 1998.

[13] T. Ghani *et al.* "100 nm Gate Length High Performance/Low Power CMOS Transistor Structure," *IEDM Technical Digest,* pp. 415-418, 1999.

[14] M. Mehrotra *et al.,* "A 1.2V, Sub-0.09um Gate Length CMOS Technology," *IEDM Technical Digest,* pp.419-422, 1999.

[15] I. Yang *et al.* "Sub-60 nm Physical Gate Length SOI CMOS," *IEDM Technical Digest,* pp.431-434, 1999.