Modeling Line Edge Roughness Effects in sub 100 Nanometer Gate Length Devices

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Abstract- **A fast method to estimate the effects of line edge roughness is proposed. This method is based upon the use of multiple 2D device "slices" sandwiched together to form an MOS transistor of a given width. This method was verified to yield an accurate representation of rough edge MOS transistors through comparisons to full three dimensional simulations. A subsequent statistical study shows how the variation in line edge roughness affects the values and variances of several key device parameters.**

I. INTRODUCTION

Current state of the art processes are able to consistently reproduce poly linewidths below 100 nm. As the linewidth is scaled down, however, the roughness on the edge of the line does not scale. The edge roughness of poly lines is typically on the order of 5 nm, but can have values much larger than that, depending on how the poly line was formed. The SIA national technology roadmap tells us that devices built at this scale are required to control gate length within approximately 8 nm [1]. Edge roughness is one of the primary concerns in controlling the gate length.

A typical image of photoresist lines and spaces shows variation along the edge of the photoresist. Figure 1 shows such edge variation. Measurements of the linewidth can be performed on such structures, and the resulting distribution of linewidths can be determined. The results of this type of measurement was performed on the lines shown in Figure 1 and are plotted in Figure 2. Although the measurement shown here is of photoresist lines, the pattern transferred to polysilicon gates shows the same or worse edge roughness than that indicated by the photoresist.

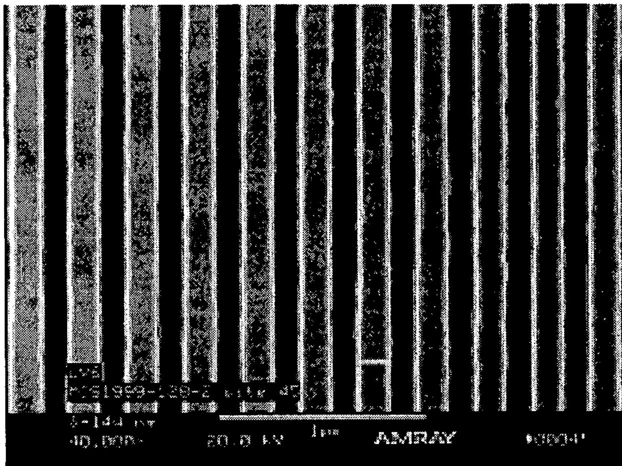

Fig. 1. Photoresist lines and spaces indicating typical edge roughness.

II. METHODOLOGY

To simulate the effect of line edge roughness (LER) on device characteristics, we assume that a 3D device with rough edges can be broken up into multiple 2D devices with different gate lengths. For a given device width, *W*, we break up a 3D structure into *N* 2D segments, add up all of the current components from the *N* different segments and divide by *N* to yield the average current through the device. With this approximation, we assume that current flows parallel to the edges of the device and there is no 3-dimensional current flow, so this is expected to be a worst case analysis.

A Monte Carlo program was written that generates a gaussian distribution of gate lengths centered around a given gate length with typical 3-σ variations. For each value of gate length generated by the program, precalculated I_d-V_g characteristics (both linear and saturation) were added together and averaged. Measurements of edge roughness on photoresist lines like those shown in Figure 1 under typical processing conditions indicated that the 3-σ edge variation is approximately 17 nm. The gaussian fit to this data is shown

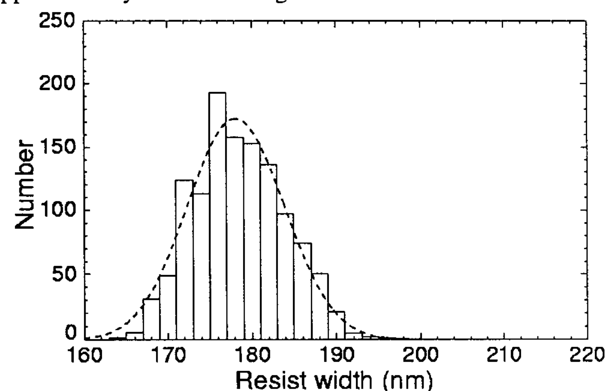

Fig. 2. Measured distribution of line width from lines and spaces shown in Figure 1 along with gaussian function used in the Monte Carlo simulation. The fit of the gaussian function is indicated by the dashed line.

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TABLE I

Effect of line edge roughness on key device parameters for an 80 nm device design.

Parameter		Device				
		no edge effect	L_{poly} σ = 5.7 nm			L_{poly} σ = 11.4 nm
			W=10 μm, w/rough edge	W=0.25 μm, w/rough edge	W=0.050 μm, w/rough edge	W=0.25 μm, w/rough edge
Vtlin (mV)	Average	300.3	298.4	298.5	298.9	289.7
	σ (3-σ var. %)	------------	0.310 (0.311)	2.087 (2.10)	5.01 (5.03)	5.08 (5.27)
Vtsat (mV)	Average	189.8	179.3	179.6	180.4	137.8
	σ (3-σ var. %)	------------	0.834 (1.40)	5.25 (8.77)	12.1 (20.0)	17.3 (37.7)
I_{off} (nA/μm)	Average	31.08	60.28	60.06	60.13	448.7
	σ (3-σ var. %)	------------	1.98 (9.84)	12.34 (61.6)	28.26 (141.0)	202.5 (135)
I_{on} (μA/μm)	Average	768	768	768	768	771
	σ (3-σ var. %)	------------	0.079 (0.308)	0.503 (1.96)	1.15 (4.50)	1.00 (3.90)

in Figure 2. Edge roughness measurements also tell us the effective width of each 2D "slice" that we use in our analysis, which is approximately 7nm. This width was determined by dividing the total length of the measured photoresist lines by the number of linewidth measurements. A better method to determine the width of each slice would be to perform a Fourier analysis of the edge roughness spectrum. This type of analysis has been performed on a variety of photoresist lines indicating spatial periods ranging from 10 nm to 50 nm or more. In this work however, we use a fixed value of 7 nm for the width of the slice.

Linear and saturated I_d-V_g characteristics were generated for a rough edge device and a shift and ratio [2] algorithm was used to extract Vtlin, Vtsat, I_{on}, and I_{off} values. This procedure was repeated using different random number seeds in the Monte Carlo program. After 5000 device parameters were extracted, averages and standard deviations were calculated.

III. Device Specifics

We define a generic sub 100 nm process with target Vtlin and Vtsat to be a few hundred millivolts, and with off and on currents to be in the few 10's of nA/μm and better than 600 μA/μm region respectively at a power supply of 1.5 V. We choose a nominal gate length of 80 nm and use a line edge roughness variance of approximately 5.7 nm. The device simulator Fielday [3] was used to generate the 2D I_d-V_g characteristics for various gate lengths. The methodology described previously was used and key device parameters were calculated. Device width was varied by using more 2D "slices" for wider devices. Because the slice width is approximately 7 nm, 7 slices were used to define a device width of 50 nm, and 1428 slices were used to define a 10 μm channel width device. Additionally, the variance in the gate edge roughness was doubled to look at changes in average values as well as variances in the obtained device parameters.

IV. Simulation Results

Table 1 summarizes the results of the calculation. For a given gate edge roughness (L_{poly} σ = 5.7 nm), we see that the average values of the various parameters are relatively independent of gate width. The variance does depend on gate width, as is expected. The variance is seen to vary as the inverse square root of the gate width. Figure 3 shows that the spread in off and on currents varies with device width. Although the average value of on current is independent of LER, the off current increases due to short channel effects.

Now compare the results from the 0.25 μm device using two different values of σ for L_{poly}. For on current and Vtlin, we see that the average values do not depend strongly on the line edge roughness. The variance of Vtlin and I_{on} scale in

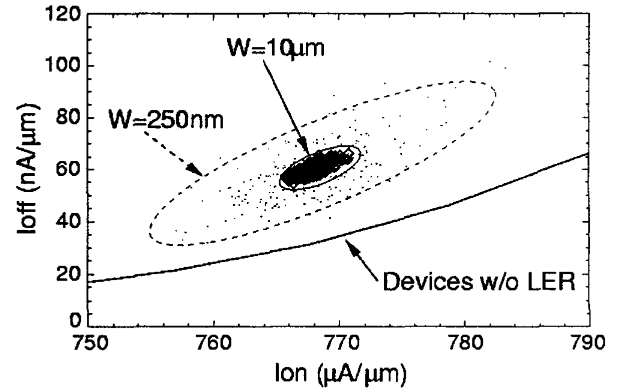

Fig. 3. Simulated spread in I_{on}-I_{off} characteristics for two device widths. The variance increases with decreasing gate width. Average on and off currents are relatively independent of gate width.

proportion to the variance in the line edge roughness. Vtsat and I_{off}, however, are very much affected by an increase in gate edge roughness. The average Vtsat is reduced by more than 40 mV, and accordingly, the average off current increases for the same device with less edge roughness by nearly an order of magnitude.

We compare this work to a study of discrete dopant effects in 50 nm wide devices [4]. LER shows a 1-σ variance in Vtsat of about 12.1 mV, while discrete doping can cause a variation of σ = 25 mV. Increasing the LER from 5.7 nm to 7.0 nm will approximately double the variance in Vtsat. Because of this, we see that LER effects cause as much variation in Vtsat as discrete dopant effects.

V. Verification of Proposed Methodology

A recent investigation of the effects of line edge roughness on device performance used 3D device modeling [5]. The structure that was utilized assumed a single step in the gate length to emulate the effects of gate edge roughness. We also defined 3D device structures with edge roughness, but we defined many more steps along both the source and drain side of the gate edge.

A. Definition of the 3D Structure

50 nm gate width devices were defined using 7 discrete gate lengths distributed randomly using the Monte Carlo program that was described earlier. The doping profiles along the device length direction were the same as that used for the 2D devices. In the gate width direction, a gaussian fall off was assumed, using a standard deviation equal to that used in the length direction (15 nm).

Using the Monte Carlo program described earlier, we defined 70 3D devices with rough edges and simulated the linear and saturated I_d-V_g characteristics using Fielday. A plot of one of the 3D device structures and the electron concentration at threshold voltage for the device in saturation is shown in Figure 4.

From these characteristics, the same device parameters were extracted as for the 2D "slice" analysis above. For the 70 3D devices, we extracted a 3-σ variation in Vtlin, Vtsat, I_{off}, and I_{on} of 5.03%, 19.3%, 107%, and 3.88% respectively compared to 5.03%, 20.0%, 141%, and 4.5% using the 2D "slice" methodology. Because the variances for the various device parameters are quite comparable, summing up I_d-V_g characteristics from multiple 2D "slices" is seen to be a valid method to estimate the effects of edge roughness.

One of the concerns addressed by 3D modeling that cannot be adequately addressed by a 2D "slice" analysis is that of asymmetry in the drain currents due to edge roughness. 20 3D devices were defined as above with the same device dimensions (W=50 nm, nominal gate length of 80 nm). I_d-V_g characteristics of the device in saturation were calculated, then the source and drain were reversed, and the same calculation was performed. Insignificant asymmetry in the currents was found even in the subthreshold region. The maximum asymmetry found was on the order of 0.3% just below threshold voltage. Above threshold, asymmetry in the drain current was found to be less than 0.05%. Since the device width that we defined was only 50 nm, for wider devices we would expect the asymmetry to be even less. This tells us that asymmetry in the device currents due to line edge roughness should not be a concern.

Comparing cpu times for the two methods, 70 3D linear and saturated I_d-V_g characteristics took approximately 3 cpu-months. In contrast, the 2D "slice" method took about an hour of cpu time to generate 5000 I_d-V_g characteristics.

B. Underdiffusion of Source/Drain Extension

For gate edge roughness that has a high spatial frequency, we would expect that lateral straggling of the extension implants and subsequent annealing would cause any roughness of the source and drain junctions to be smoothed out by diffusion. For the doping profile of the 3D devices shown in this work, we assume that the edge of the source and drain extension regions follow the gate edge roughness. We have, however, defined the doping profiles in the depth direction such that the extension doping profile and junction transition smoothly from one gate step to the next. This is a reasonable assumption if the extension implant energies are low and the thermal budget is small. It is also a valid assumption if the spatial frequency of the steps is large compared to the thermal budget.

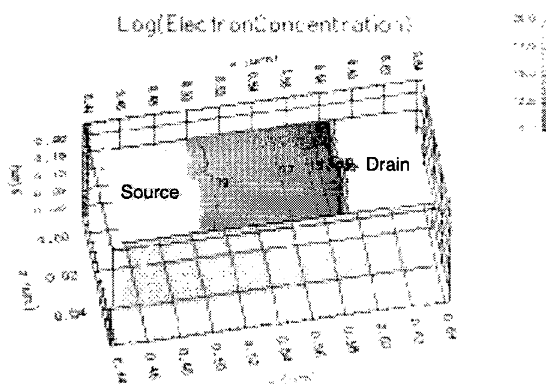

Fig. 4. Equicontour lines of electron concentration at the silicon surface for a 50 nm channel width 3D device with line edge roughness. The drain was biased to 1.5V and the gate voltage was near the threshold voltage. The edge roughness of the gate can also be seen.

We can estimate the thermal budget required to swamp out edge roughness of the source and drain junctions due to poly gate edge roughness by defining a cross-sectional area of a gate edge, A_{diff} to be equal to the thermal budget, *Dt*. A_{diff} can be estimated to be the spatial frequency of the edge roughness times the 3-σ variation in gate edge roughness. For the device that we defined above, $A_{diff} = 15nm \cdot 14nm = 210nm^2$. For a low energy 6 keV Arsenic implant, the thermal budget needed to cause extension implants to be smoothed out under the gate edge would be greater than 20 seconds at 900C (assuming a diffusivity of ~10 nm^2/sec). For larger spatial frequencies, longer anneal times would be needed. Increasing thermal budget to reduce the effects of gate edge roughness on extension junction roughness is not a desired option, since thermal budgets are increasingly being reduced in order to allow for steeper doping profiles.

VI. Conclusions

A fast method for determining the effects of line edge roughness on device performance was shown to be valid based on a comparison to full 3D device modeling. A quantitative analysis showed how line edge roughness affects device parameters for a sub 100 nm device design. LER effects can cause as much or more variation in device performance as discrete dopant effects. Although I_d-V_g characteristics from 2D device simulations were used in this analysis, an even more significant savings in cpu time can be realized by utilizing I_d-V_g characteristics generated from compact models.

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