CHAMPS (CHemicAl-Mechanical Planarization Simulator)

Yoo-Hyon Kim, Kwang-Jae Yoo, Kyung-Hyun Kim*, Bo-Yeon Yoon*,
Young-Kwan Park, Sang-Rok Ha*, and Jeong-Taek Kong
CAE, *Process Development Team, Semiconductor R&D Center, Samsung Electronics Co., Ltd.
San #24 Nongseo-Ri, Kiheung-Eup, Yongin-Shi, Kyungki-Do, Korea
E-mail : yoohkim@samsung.co.kr, Phone : +82-2-760-6248, Fax : +82-2-760-6259

***Abstract*—Simulation of chemical-mechanical polishing is important because the chip-level planarity and wafer-level unformity dependent on many dynamic factors are difficult to control. CHAMPS (CHemicAl Mechanical Planarization Simulator) has been developed for predicting and optimizing the thickness distribution after the CMP process using the chip-level pattern density and an elastic spring model including equipment parameters. In this work, the results of CMP simulation is shown to agree well with the measured data. This simulator can be used to optimize CMP process conditions and to generate design rules for filling dummy patterns which are used to improve the planarity and uniformity.**

I. Introduction

In chemical-mechanical polishing (CMP), the global planarity is dependent on many dynamic factors (i.e., layout, feature size, pattern density, film material, deposition process, etc.). CMP factors include: time, pressure, velocity, temperature, slurry feed rate, polishing motion, slurry chemistry a pH potential, slurry particle size, carrier film, pad hardness and pad conditioning method, among others. Therefore, simulation modeling is getting more important to cover dynamic factors effectively and to predict topography after CMP including above factors and to understand the mechanisms such as the relationship between the stress and the polishing removal rate. Although many simulation approaches have been introduced in CMP modeling so far [1], [6], there has been no attempt to establish the systematic simulator from the feature level to the wafer level including layout modification.

II. Feature of CHAMPS

Fig. 1 depicts the simulation flow in the CHAMPS system. It consists of three levels in a CMP process: wafer level, chip level, and feature level [4]. The chip level simulation responses to the question of local planarity and it is the most important part. One major application is to establish the monitoring points from the surrounding pattern density map in a chip. Another is to help optimizing the design of dummy patterns. By adding dummy patterns to the initial design, one can check the CMP results using a predictive simulation. In other words, the process of "trial-and-error" is mainly performed on a computer. Therefore, the amount of the total turn around time in real fabrication and the design cycle can be shortened. We have found that the pattern density of the surrounding cells by convolving the nonlinear weighted function is closely related with the ILD thickness distribution. This nonlinear weighted surrouding pattern density map of a chip can be applied to extract

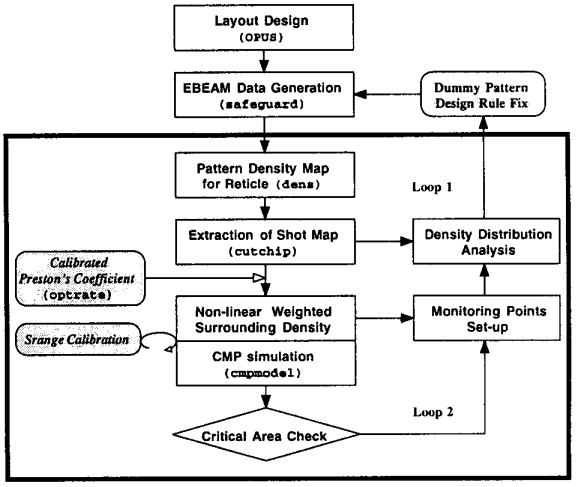

Fig. 1. The CMP simulation flow of CHAMPS.

monitoring points for the CMP process control.

A. Pattern Density

The strong dependence between the underlying pattern density and the ILD thickness is well recognized for CMP, and it has been demontrated that the pattern density is the primary variable controlling CMP-induced ILD thickness variation at the chip level [2], [3]. The local pattern density, $\rho_0(i,j)$, can be defined as the volume fraction of the deposited film within an infinitesimally thin wafer surface. The entire chip is divided into square unit cells, where the number of cells and scaling factor are input variables. When a chip layout is read in, the local pattern densities of each cell are accurately calculated by identifying the local pattern and generates the pattern density map of a chip. Since the calculation time of this pattern density is very critical to simulating the CMP process, we reduce the time dramatically using the e-beam data as shown in Fig. 2. The pattern layout has to be in e-beam data, which is the most common pattern file format of the MEBES e-beam writing system. Even though graphical design system (GDS) II stream format may be used as the alternative layout input format, it may be too slow for layout analysis and pattern density calculation. However, it is noted that the profile after deposition cannot always be approximated by the underlying layout pattern density. Especially, the pattern density of the region with the tightest pitches or small features is very different from the underlying layout due to the deposition profiles. Owing to this reason, the computation of the local pattern density due to the

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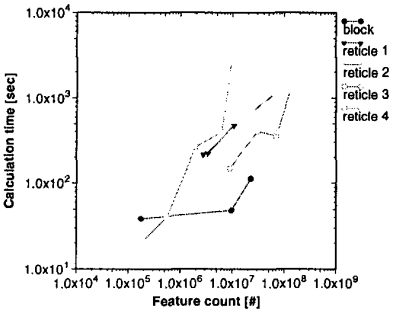


Fig. 2. CPU times vs. feature counts.

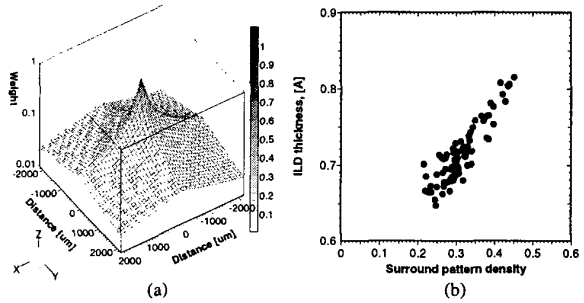


Fig. 3. (a) Nonlinear weighted function. (b) Relationship between the nonlinear weighted surrounding pattern density and the ILD thickness after a CMP process.

pattern bias effect also depends on accurate deposition profiles, equipments, and materials which are an important modeling issue in CMP.

As mentioned in [6], the effective pattern density is an important concept in CMP modeling. We have found intuitively that the pattern density, $\rho_s(i,j)$, of the surrounding cells by convolving the nonlinear weighted function is closely related with the ILD thickness distribution as shown in Fig. 3 (b).

$$\rho_s(i,j) = \frac{1}{(2m+1)^2} \sum_{l=-m}^{m} \sum_{k=-m}^{m} \frac{\rho_0(l,k)}{(|l|+|k|)} \cdot \rho_0(i,j), \quad \text{when } l,k = 0,\ m = 0.5 \tag{1}$$

where $2m+1$ is the number of surrounding cells in one side length of the surround density window. l and k are the number of cells from the origin of unit cell (i,j). When the pattern is completely filled, i.e., the bare wafer, the nonlinear weighted function is shown in Fig. 3 (a). *Srange* is defined as $(2m+1)$ times the dimension of the squared unit cell. Consequently, the nonlinear weighted surrounding map according to *Srange* is interpreted by an intuitive physical insight as the region over which the pad bends and conforms to the wafer surface. *Srange* is typically in the order of several millimeters in the oxide ILD CMP case [7].

B. CMP Simulation Model

In order to consider the equipment parameters, such as down pressure, relative rotation speed, pad thickness and modulus, simple elastic spring models have been introduced [2], [5]. This model consists of three basic equations. They are the Preston's equation, the elastic spring pad, and the mean pressure distribution.

$$\frac{dX_u}{dt} = k \cdot P_u \cdot V, \quad \frac{dX_d}{dt} = k \cdot P_d \cdot V \tag{2}$$

$$P_u - P_d = \frac{E}{U}(X_u - X_d) \tag{3}$$

$$\rho P_u + (1-\rho)P_d = P \tag{4}$$

where dX_i/dt is the polishing rate of the up features X_u and the down features X_d, P_u is the pressure at the up features and P_d is the pressure at the down features, V is the relative velocity between the wafer and the polishing pad, and k is the Preston's coefficient incorporating both chemical and mechanical components. E is Young's modulus and U is the thickness of a pad in (3). The average pressure P is the sum of the partial pressure P_u and P_d with pattern densities ρ and $(1-\rho)$ in (4). Modification is required if the polished layers are multiple as in polishing, such as shallow trench isolation and damascene processes.

Since the fundamental mechanism of k is very complicated, this is still a matter of reserch and further modeling work. In CHAMPS, the following empirical form is introduced. From the experiment of the polishing rate of plasma-enhanced chemical vapor deposition tetraethylorthosilicate (PE-TEOS) deposited on flat wafers without topography, it is found that k is a function of the pressure and relative rotation speed. The coefficient could be described by an empirical curve fitting dependent on the down pressure and relative rotation speed.

$$k(P,V) = [\alpha + \beta \exp(-\gamma P)] \cdot [\exp(-\eta V)] \tag{5}$$

where α, β, γ, and η are estimated from the fitting curve, respectively. The estimated value of α, β, γ, and η are 2.0×10^{-13}, 0.8×10^{-13}, 9.7×10^{-5}, and 0.55 for PE-TEOS, respectively. The value of the coefficient decreases as the down pressure and platen speed become higher. The chemical effects encapsulated in k include the chemical reactions between the slurry and the wafer as well as the availability of the slurry at the wafer surface. Therefore, just as the slurry type and wafer surface will be affected by k, so will the pad's ability to deliver the slurry to the wafer surface. This coefficient is a strong function of the equipment conditions and consumables.

Finally, assuming the thickness from the under layer to the top in the unit cell (i,j) is described by $H(i,j) = \rho_0 X_u + (1-\rho_0)X_d$, the final height of $H(i,j)$ after CMP as follows:

$$H(i,j) = X_0(i,j) - kVPt + h_0 \left\{ \rho_0(i,j) \exp^{(-\frac{kVE}{U}t)} + \rho_s(i,j) \left[1 - \exp^{(-\frac{kVE}{U}t)} \right] \right\} \tag{6}$$

where the second term in the right side is the polished thickness of a bare wafer, and the third therm is the step height at each time iteration. Three main parameters which are the Preston's coefficient, *Srange* and scaling factor need be calibrated to create a successful chip-level CMP simulation.

At the wafer level, the same model equation is used except the bare-wafer polishing rate and the boundary condition. In other words, the polishing rate is dependent on the position of wafer. Although P may also vary across the wafer surface, its distribution is better known. Specifically, P's average value

TABLE I

Design Parameters And Its Optimized Value By Statistical Analysis.

Parameter	Unit	ΔX	Center	Max.	Min.	Found
$Srange$	$[um]$	± 1000	2000	4000	0	2566.0
$Tpad$	$[mil]$	± 30	80	140	20	51.74
$Epad$	$[psi]$	± 200	400	800	0	549.50
$szCell$	$[um]$	± 100	300	500	100	292.58

can be computed by dividing the process down-force by the wafer size. Other factors such as the curvature of the wafer backing film and positions of vacuum holes provide information regarding how P may be distributed across the wafer. The shape of the pressure distribution, based on such information, can be approximated using various functions and corresponding fitting parameters. The model discussed here which admits a wafer-centered quadratic pressure distribution is adopted [8]. The shape of the distribution is expressed as

$$P_q(r) = P_i - (P_i - 1)\left(\frac{r}{R_w}\right)^2 \tag{8}$$

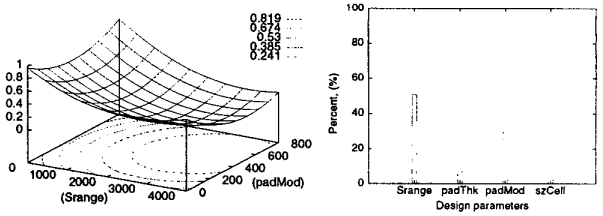
where r is the distance from the wafer center, R_w is the radius of the wafer, and P_i is the pressure at the wafer center relative to the wafer edge. Another important parameter is the boundary condition for the edge of a chip. In simulation, the neighbor section of the edge is divided by 8. The density condition outside the chip area is considered according to the periodic chip boundary condition or the pattern density due to photoresist type. For example, in the case of a positive resist, the density is 0, otherwise, the density is 1 for negative resist. Additionally, when the surrounding cells are out of wafer edge exclusion, the density is definded as 0.

C. Model parameter calibration

Design centering is one of the optimization methodologies used to obtain the maximum VLSI yield under specified circuit performance. This methodology can be widely applied to many different step for optimum VLSI design, such as process, device, and circuit designs and simulator model tuning [9]. The goal is to extract optimum model parameters in CHAMPS to match measurements of the step height and the layer thickness. SECRSM, an in-house developed software, is used to the calibration by statistical analysis.

Four model parameters which are surround range $Srange$, pad thickness $Tpad$, pad modulus $Epad$, and the unit cell size of local pattern density map $szCell$ were chosen. The thickness after a CMP process (objective target) were chosen and details of the above values, definitions, and units are listed in Table I. Twenty-five different conditions were obtained when four model parameters were designated. This matrix is generated by the central composite method based on the theory of design of experiment. Step heights on the square box pattern after 60 and 150 sec CMP were simulated by CHAMPS. Regression models of the time-dependent step height as a function of the CHAMPS model parameters were constructed. Estimators of regression models were derived. From these results, step height characteristics are expressed by quardratic expressions. The accuracy of these quardratic expressions was confirmed by the estimated error.

Optimization is performed using response surface models to find model parameters that achive the best fit to experimental data. The optimum model parameters, which minimize a combined object function, were obtained according to the feature size by 25 different initial values as shown in Table I. A comparision between the step heights from mesurements, simulation before calibration, and simulation after calibration is given in Fig. 4 (a). The model parameter sensitivity P_k for Y_k is defined as follows:



(a) (b)

Fig. 4. (a) A comparision between the step heights from mesurements, simulation before calibration, and simulation after calibration. (b) The model parameter sensitivity using statistical analysis.

$$P_k = \sqrt{\sum_{i=1}^{4} \Delta Y_{ik}^2 / Y_{sk}} \tag{9}$$

where $\Delta Y_{ik} = Y_{ik\max} - Y_{ik\min}$, $Y_{ik\max}$ and $Y_{ik\min}$ are maximum and minimum values of Y_{ik} between $X_i = -2$ and 2. In Fig. 4 (b), the result of model parameter sensitivity is shown.

III. Results

On wafers, a 8000 Å thick metal stack layer was deposited. The wafers were patterned with a metal 1 mask and DUV lithography. After etching and stripping, the ILD layer was deposited by a 6000 Å high density plasma (HDP) CVD oxide and a 15000 Å TEOS. The initial step height is 0.8 μm and the layer thickness is 2.098 μm. The measurement data was obtained from wafers polished during 170 sec on a CMP machine, using a K-grooved IC1000/SUBA IV pre-stacked pad, Semi-Sperse 25 slurry, 8.5 psi down pressure, 35 rpm platen speed, and 15 rpm carrier speed. The removal rate for the planarization process was 2800 Å/min which was first determined on a blanket wafer. The parameters for Preston's coefficent are used in the calibrated values for the TEOS material. Measurement scans of the film thickness were taken on the metal pattern using Opti-Probe 2600.

Fig. 5 (a) illustrats the pattern density map and the 83 points for monitoring the layer thickness variation at the chip level. The total cell number is $201 \times 198 = 39,798$ and the area of the unit cell is $99.5 \times 99.5\ \mu m^2$. The average pattern density is 29%. In this simulation, we assume that the initial thickness of under metal layer is flat though the thickness variation of TEOS layer at the top height is about 641 Å from measurement. Fig. 5 (b) shows the remained layer thickness by CMP simulation, the maximum height is 8443 Å, the minimum is 6110 Å, and the average is 7117 Å. It also shows that the step height is almost linearly reduced before the initial feature steps are completely eliminated and then not easily reduced. The measured and simulated heights at monitoring points, and the tendency of the variation are quite well matched. The average error of simulation is 2.1% and the maximum error is 9.6% as shown in Fig. 5 (c).

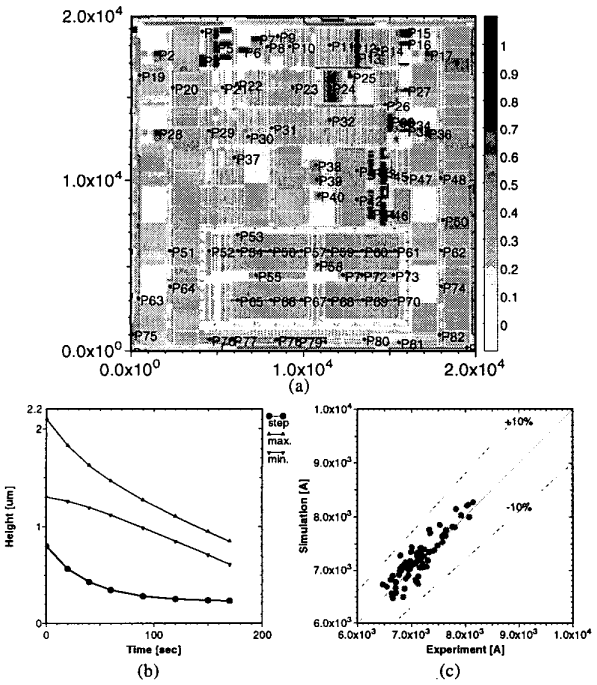


Fig. 5. (a) The local pattern density map of metal 1 layout and 83 monitoring points. (b) The time-dependent maximum, minimum and its step height by simulation. (c) The comparision between simulation and experiment for the layer thickness after a CMP process.

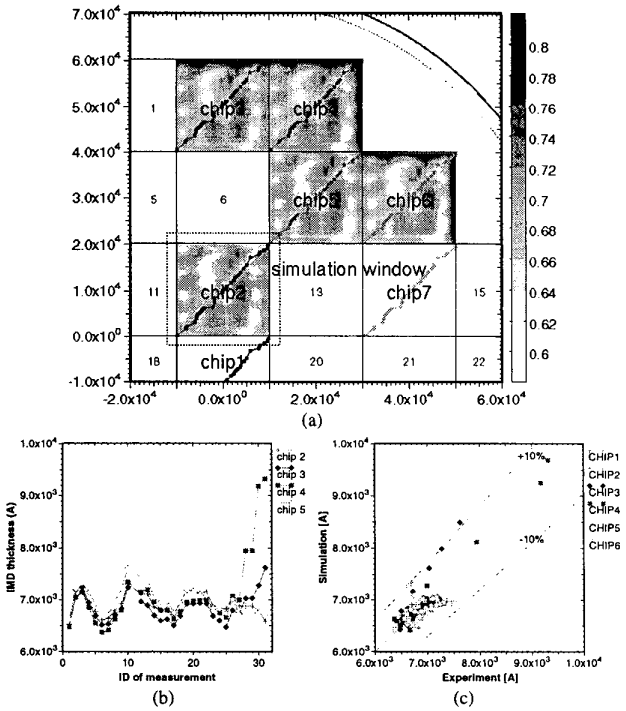


Fig. 6. (a) The wafer-level CMP simulation results. The placement of chip in the wafer and the monitoring points for layer thickness within each chip. (b) Experimental layer thickness within each chip. (c) CMP simulation and experimental result of wafer level.

In order to investigate the uniformity and planarity, 31 points of a diagonal direction are scaned within 7 chips located in the top right wafer region as shown in Fig. 6 (a). In this experiment, the dummy photo shot is not exposed at the wafer edge. Therefore, the wafer region except chip areas is unpatterned and the pattern density can be treated as 100% due to the positive photoresist. As shown in Fig. 6 (b), the planarity is significantly different at the top right chips because of the edge boundary condition. This difference begins to change from the 27th monitoring point, but the remaining sites below this point have the nearly same trend in the thickness variation. This point is located at 2 mm in x-direction and 3 mm in y-direction from the top right edge of the shot. Thus, we can deduce that the planarization length is similar with the distance from this point to the corner of the chip. The number 4 and number 6 chips have two opened sides and the unpolished amount is the largest at the top right corner of the chip.

IV. Conclusions

In this paper, we have described CHAMPS which performs the process simulation of CMP including issues from equipment to design. Through this method, we can extract the design rules and equipment conditions to improve the yield. In addition, to meet the requirements of rapid computation, CHAMPS takes advantage of the architecture and data format of input layout. Therefore, fine tuning of the layout through a closer interface of the design to the process phase is worthwhile. Furthermore, an integration of process simulators with layout tools can be used to evaluate the limits of new nonconventional process techniques, in the early process definition stage.

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