An Analysis of Program and Erase Operation for FC-SGT Flash Memory Cells

Masakazu Hioki[1)], Tetsuo Endoh[1)], Hiroshi Sakuraba[1)], Markus Lenski[1)] and Fujio Masuoka[1)]
[1)] Research Institute of Electrical Communication, Tohoku University
2-1-1 Katahira, Aoba-ku, Sendai 980-8577, Japan

Abstract— **The floating channel type surrounding gate transistor (FC-SGT) Flash memory cell realizes high-speed bipolarity program and erase operations. In the current investigation, the time dependence of the surface potential in the floating channel region, which strongly affects program and erase performance, is studied during program and erase operation. By analyzing the carrier generation processes in floating channel region, the program and erase operation for FC-SGT Flash memory cell is made clear.**

I. Introduction

High-packing density, low-power operation, high-speed program and erase operations and high-reliability are nowadays required in state-of-the-art Flash memory devices [1]. Three-dimensional structured cells offer high-packing densities, while bipolarity program and erase operation modes are compliant with low-power operation providing high speed and high reliability. In order to realize the above mentioned requirements, Floating Channel type Surrounding Gate Transistor (FC-SGT) Flash memory cell has been proposed [2][3]. The FC-SGT structure is shown in Fig.1. Drain, source, and channel region are arranged vertically with respect to the substrate. Tunnel oxide, floating gate, interpoly insulator, and control gate surround the silicon pillar. The channel region in this structure is floating. The program and erase performance has been reported [2]. It has been shown that the program speed is twice as high as compared to a planar type Flash memory cell. As expected, the surface potential in the floating channel region greatly influences the program and erase characteristics during operation. In this paper, the physical mechanisms contributing to the time-dependence of the surface potential during program and erase operation are analyzed and discussed.

II. Program and erase characteristics

Program operation is performed by applying a high positive voltage V_P to the control gate, while source and drain are set to 0V (Fig.2(a)). Under these conditions, electrons are injected by FN tunneling from drain, source and inversion layer to the floating gate, hereby causing a positive shift of the threshold voltage (Fig.3(a)). Erase operation is performed by applying 0V to the control gate, and by setting source and drain to a high positive voltage V_E (Fig.2(b)). Under these conditions, electrons are emitted by FN tunneling from the floating gate to drain, source and floating channel region. In this case, the threshold voltage decreases as a function of the erase time (Fig.3(b)). While the surface potential during program is time-independent (Fig.3(a)), the opposite holds during erase (Fig.3(b)) showing a complex dependence of the surface potential on erase time. This transient behavior during erase is determined by the overall capacitance network of the device consisting of pn-junctions, tunnel oxide, interpoly insulator, and the total charge density in the channel region (Fig.4). The charge in the channel region originates from leakage currents through the pn-junctions and from FN injection currents through the tunnel oxide. The time-dependence of the surface potential in the floating channel region is simulated by using a 2-D device simulator [4]. Herein, special attention is paid to several carrier generation processes, which contribute to charge built-up in the channel region. Fig.5 shows a schematic view of the several carrier generation processes, which have been taken into consideration for the erase operation. The leakage currents at the pn-junctions are assumed to consist of two carrier generation processes: (1) Impact ionization in the depletion region, (2) band-to-band tunneling in the corner-overlap region of tunnel oxide and n-type diffusion, and (3) the electron flow originating from the floating gate by Fowler-Nordheim tunneling.

III. Results and Discussion

In the device simulation, the above given contributions were separately taken into account and compared with the final, resulting transient surface channel potential during erase operation. Neglecting carrier generation processes, Fig.6 shows that the surface potential raises until 0.1ns up to 10V, and remains constant for longer erase times. Including carrier generation by impact ionization (II) leads to an additional increase of the surface potential of 2V to 12V for erase times longer than 0.1ns (compared to the preceding one). Including band-to-band tunneling (BBT) gives rise to an additional increase in the surface potential, which only slowly tends to saturate in the time domain considered herein. Finally, the surface potential achieves the same value as of source/drain for erase times greater than 10μs, when the charge build-up by FN-tunneling (FN) is included.

IV. Conclusions

The surface potential of the floating channel region, which strongly affects the erase characteristics of FC-SGT Flash memory, exhibits a complex time-dependence during erase operation, while the surface potential during program operation is time-independent. The rapid, additional build-up of the surface potential of the floating channel region for short erase times (< 0.1ns) is caused by carrier generation due to impact ionization (II) in the depletion region of source/drain and floating channel (Fig.6).

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For longer erase times (> 0.1ns) band-to-band tunneling (BBT) contributes to a further increase in the surface potential. Finally, charge generation by FN-tunneling (FN) is the slowest process considered herein and is negligible for erase times shorter than $10\mu s$. From above all, program and erase operation for FC-SGT Flash memory cell has been clarified.

Acknowledgements

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References

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TABLE I
DEVICE PARAMETERS.

L	Gate length	$1\mu m$
R	Silicon pillar's radius	$0.2\mu m$
T_{oxI}	Thickness of interpoly insulator	20nm
T_{oxT}	Thickness of tunnel oxide	10nm
N_D	Impurity concentration of drain/source	$10^{20}1/cm^3$
N_A	Impurity concentration of channel region	$10^{18}1/cm^3$
$C_I(=C_I/C_T)$	Coupling ratio	1

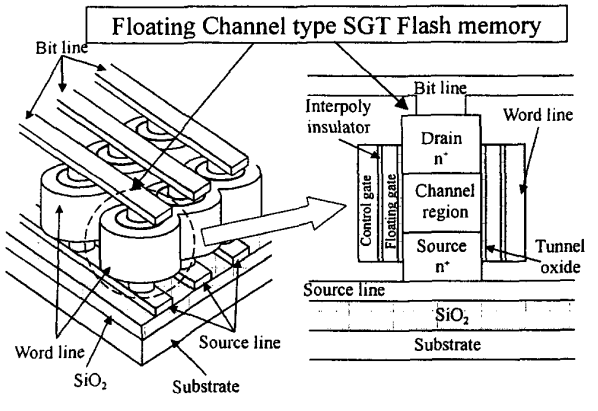

Fig. 1. The structure of FC-SGT Flash memory cell.

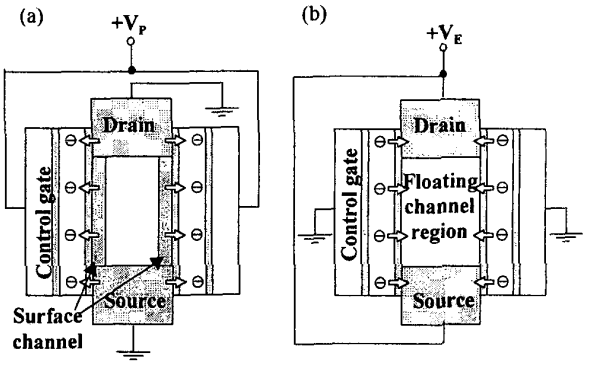

Fig. 2. Bias conditions during (a) program operation and (b) erase operation.

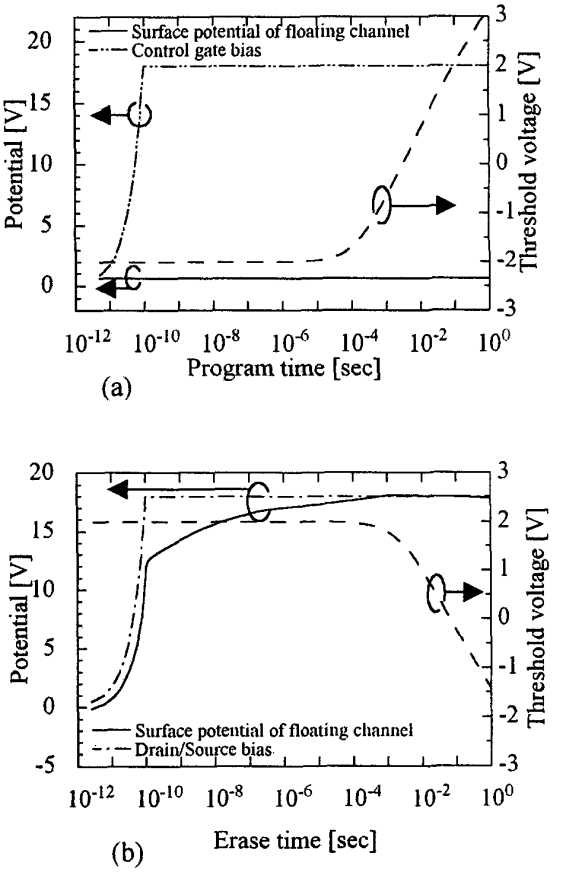

Fig. 3. Surface potential of the channel region and threshold voltage during (a) program operation (b) erase operation.

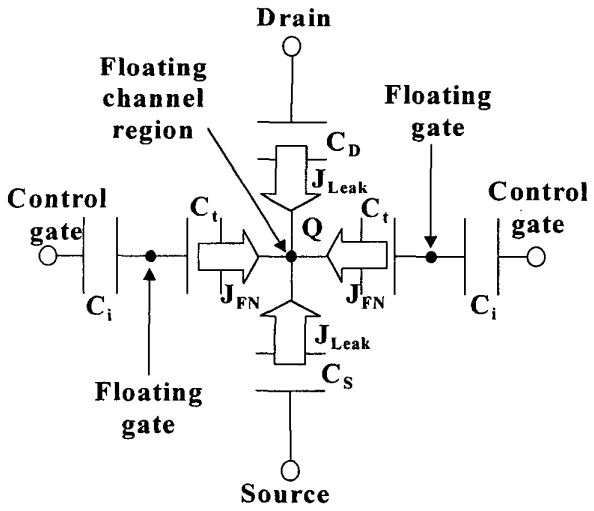

Fig. 4. Equivalent circuit during erase operation.

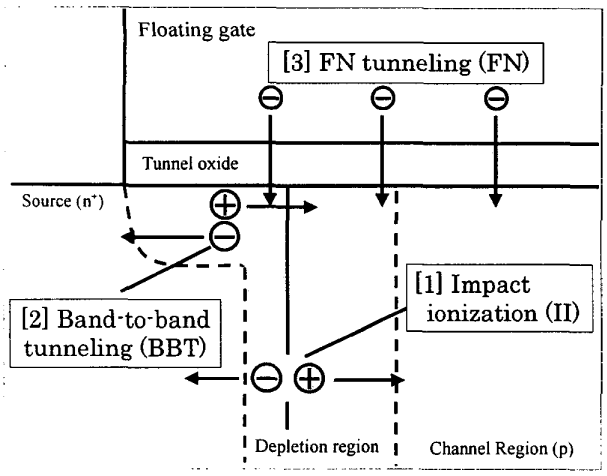

Fig. 5. Carrier generation processes during erase operation.

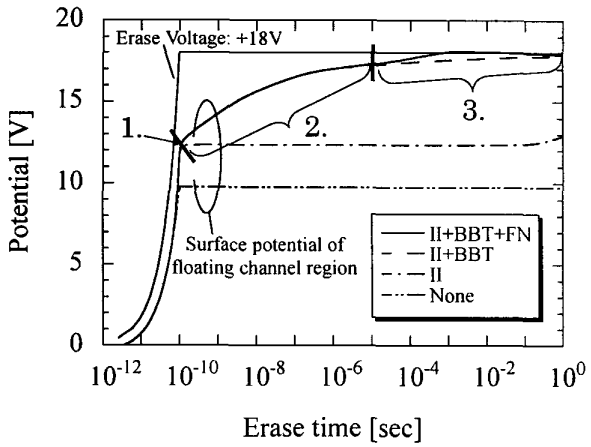

Fig. 6. The relation between surface potential and carrier generation processes (II: Impact ionization, BBT: Band-to-band tunneling, FN: FN tunneling, None: No carrier generation processes).