Comprehensive Analytical Charge Control and I-V Model of Modern MOSFET's by Fully Comprising Quantum Mechanical Effects

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Abstract: A new analytical charge control and I-V model for sub-micron and deep sub-micron MOSFET's is developed based on a newly developed charge control model in MOS structure. Threshold voltage shift due to Quantum Mechanical Effects (QMEs), finite inversion layer thickness effect (inversion layer capacitance) as well as increase of depletion layer charge density after the strong inversion point are cooperated in the model.

1. Introduction

As the development of MOS ULSI technology, the basic element of ULSI has been scaled down to sub-micron and deep sub-micron regimes. Analytical MOSFET's I-V model for circuit simulator is necessary to meet the requirement of circuit design. Generally speaking, there are two requirements regarding the analytical model. One is physically-based, the other is continuity between different operation regions. As for the physically based aspect, the Quantum Mechanical Effects (QMEs) in MOS inversion layer are not included in most published models [1,2]. Since the Quantum Mechanical Effects (QMEs) have significant influences on threshold voltage [3], on gate capacitance attenuation [4] due to finite inversion layer thickness, on current drive capacitance and transconductance degradation [5], it is not physically-based if QMEs are not included in a model.

In this paper, a newly developed, closed-form comprehensive charge-voltage model of MOS inversion layer is presented. Explicit expressions of surface potential and inversion layer charge sheet density for the whole gate bias regimes with smooth transition characteristics are derived. QMEs are included in the present model in three aspects: threshold voltage shift due to QMEs following our recent work [6], the finite inversion layer thickness, and the increase of depletion layer charge after the strong inversion point due to increased surface potential. Based on the charge model a new drain current formula is developed. Channel length modulation (CLM), drain-induced barrier lowering (DIBL), mobility degradation, carrier velocity saturation effects as well as poly-silicon depletion effects are included. The model results are compared with experiment data for a large range of gate length from sub-micron to deep sub-micron meter and even for sub-100nm devices. The accuracy and scalability of the model is demonstrated.

2. Charge Control Model Comprising QMEs

In this section, the inversion layer thickness and then the increased depletion charge density are modeled based on numerical results of self-consistent solution of Schrodinger and Poisson equations. And then the surface potential as well as the carrier sheet density with respect to gate potential is formulated. The inversion charge capacitance is given by:

$$C_{inv} = \varepsilon_0 \varepsilon_{s_i} / X_{dc}, \tag{1}$$

where X_{dc} is the inversion layer thickness:

$$X_{dc} = \int x \cdot n(x) dx \Big/ \int n(x) dx. \tag{2}$$

$n(x)$ is the carrier concentration at point x. It is reasonable to expect that X_{dc} is a universal function of the effective electric field in inversion layer defined as[7]:

$$E_{eff} = \left(V_{gtx} + \alpha \cdot (V_{th} - V_{FB} - \phi_{s0})\right) / 2 \cdot T_{ox} \tag{3}$$

where α is weighting coefficient. V_{th} is threshold voltage, V_{FB} is flatband voltage and ϕ_{s0} is the surface potential at the threshold point. T_{ox} is the gate oxide thickness. V_{gtx} is given by [7]:

$$V_{gtx} = \eta \cdot \phi_t \cdot \ln\left(1 + \exp\left(\left(V_{gate} - V_{th}\right)/\eta \cdot \phi_t\right)\right), \tag{4}$$

where η is the subthreshold swing parameter, ϕ_t is the thermal voltage. Based on the numerical results by solving Schrodinger and Poisson equations self-consistently, the inversion layer thickness is modeled as:

$$X_{dc} = \left(b_1 + b_2 \cdot E_{eff}\right) / \left(b_3 + E_{eff}\right), \tag{5}$$

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where the unit of E_{eff} is MV/cm. $b_1(5.047)$, $b_2(0.771)$ and $b_3(0.113)$ are determined by fitting the numerical results. The numerical and model results of X_{dc} are shown in Fig.1.

With the increase of the thickness of quantized inversion layer, the depletion charge increases at the same time. The increment of depletion charge after strong inversion is modeled below.

Since the total depletion charge is directly related with the surface potential induced by depletion charge ϕ_{s_dep} as given below:

$$Q_{dep} = \sqrt{2q_0\varepsilon_0\varepsilon_{si}\cdot N_{sub}\cdot\phi_{s\_dep}}, \quad (6)$$

where N_{sub} is substrate doping concentration, q_0 is the electron charge, we try to model the overall ϕ_{s_dep} as:

$$\phi_{s\_dep} = \phi_{s\_weak} + \phi_{s\_inc}, \quad (7)$$

where ϕ_{s_weak} is the surface potential before strong inversion as in conventional model:

$$\phi_{s\_weak} = \begin{cases} \left(\left(\sqrt{b^2 - 4\times V_{gate}} - b\right)/2\right)^2, & if\left(V_{gate} < V_{th}\right) \\ \left(\left(\sqrt{b^2 - 4\times V_{th}} - b\right)/2\right)^2, & if\left(V_{gate} > V_{th}\right) \end{cases} \quad (8)$$

with $b = \sqrt{2\times\varepsilon_{si}\cdot N_{sub}\cdot q_0/\varepsilon_0}\cdot T_{ox}/\varepsilon_{SiO2}$.

In order to get a smooth ϕ_{s_weak}, we define $V_{g\_weak} = f - \sqrt{f^2 - V_{gate}\cdot V_{th}}$ with $f = 0.5\times\left(V_{gate} + (1+\delta)\cdot V_{th}\right)$. δ is a small quantity. Thus ϕ_{s_weak} can be expressed as a unified function of V_{g_weak}:

$$\phi_{s\_weak} = \left(\left(\sqrt{b^2 - 4\times V_{g\_weak}} - b\right)/2\right)^2 \quad (9)$$

Based on the analysis of the underlying physics and by the aid of numerical results, the additional increment of surface potential due to the depletion charge is modeled as:

$$\phi_{s\_inc} = a_1\times\left(C_{gate}\cdot V_{gtx}/Q_{dep0}\right)/\left(1 + a_2\times C_{gate}\cdot V_{gtx}/Q_{dep0}\right) \quad (10)$$

where Q_{dep0} is the depletion charge at the strong inversion point. C_{gate} is the total gate capacitance. $a_1 = 1.55$ and $a_2 = 10$ are determined by fitting the model results with the numerical results.

The modeled depletion charge Q_{dep} (6) and the numerical results by solving Schrodinger and Poisson equations are shown in Fig.2. It is shown that for a large range of substrate doping levels (from $3\times10^{16}cm^{-3}$ to $3\times10^{18}cm^{-3}$) and gate oxide thickness (from 1.5nm to 7nm), the model results are coincident with numerical results very well. It is clearly

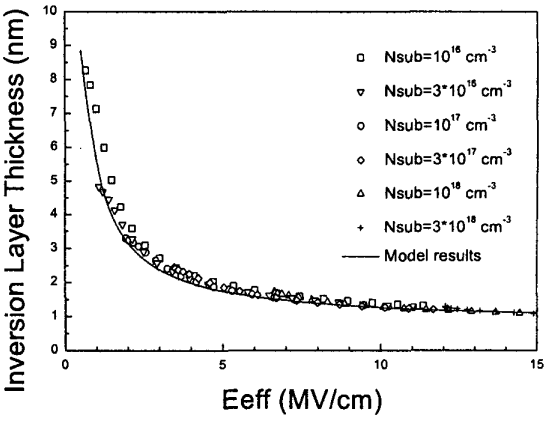

Fig.1: Inversion layer thickness with respect to effective electric filed. Symbols represent numerical results by self-consistent solution of Schrodinger and Poisson equations. Line represents model results.

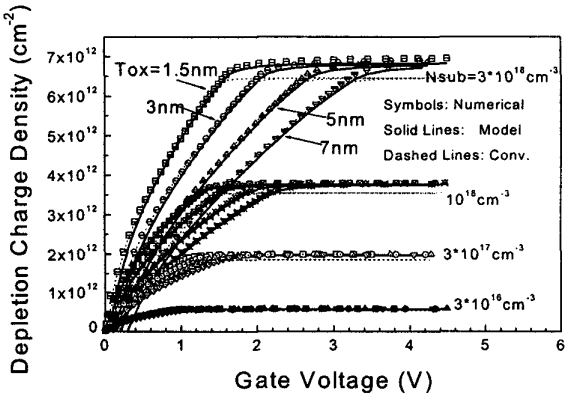

Fig.2: The depletion charge density with respect to gate voltage. Conventional model results without consideration of the increment of depletion charge after strong inversion are shown by dashed lines.

shown that when substrate doping levels are high, the errors induced by omitting the influence of ϕ_{s_inc} are non-negligible.

The threshold voltage in the above calculations are comprised of a conventional threshold voltage term and an additional quantum mechanical shift term [6] given by:

$$V_{th} = V_{th\_conv} + V_{th\_shift} \quad (11)$$

From the above results for Q_{dep} (C_{dep}) and C_{inv}, surface potential and then carrier sheet density in inversion layer are derived based on the new concept of Space Charge Capacitance (SCC):

$$C_{charge} = (Q_{inv} + Q_{dep})/(Q_{inv}/C_{inv} + Q_{dep}/C_{dep}) \quad (12)$$

Thus, the total gate charge of MOS structure can be given as:

$$C_{gate} = C_{ox} \cdot C_{charge} / \left(C_{ox} + C_{charge}\right) \quad (13)$$

The surface potential is then given by:

$$\phi_s = C_{ox} \cdot V_{gate} / \left(C_{ox} + C_{charge}\right) \quad (14)$$

The inversion layer charge density is:

$$Q_{inv} = C_{ox} \cdot C_{charge} \cdot V_{gate} / \left(C_{ox} + C_{charge}\right) - Q_{dep} \quad (15)$$

In order to get rid of the coupling of (12) and (15), Q_{inv} in (12) is approximated by: $Q_{inv} = C_{oxeff} \cdot V_{gtx}$. Where $C_{oxeff} = C_{ox} \cdot C_{inv} / \left(C_{ox} + C_{inv}\right)$.

Though the concept of Space Charge Capacitance (SCC) is applicable in all the bias regions in MOS structures, it is of no sense to model the inversion layer thickness and then the overall SCC in depletion and weak inversion region. Alternatively, we adopt the well-known formula for carrier sheet density in sub-threshold region [1]:

$$Q_{inv\_sub} = \sqrt{2 \times \varepsilon_0 \varepsilon_{si} \cdot N_{sub} / (2 \times \phi_{s0})} \cdot \phi_t \cdot \exp\left(\left(V_{gate} - V_{th} - V_{off}\right) / (\eta \cdot \phi_t)\right) \quad (16)$$

In order to get a unified formula of charge sheet density from subthreshold to strong inversion region, we introduce the effective gate voltage as:

$$V_{gsteff} = \frac{2 \cdot \eta \cdot \phi_t \cdot \ln\left(1 + \exp\left(\frac{V_{gate} - \phi_s - Q_{dep}/C_{ox}}{2 \cdot \eta \cdot \phi_t}\right)\right)}{1 + 2 \cdot \eta \cdot C_{ox} \sqrt{\frac{2 \cdot \phi_{s0}}{q_0 \cdot \varepsilon_0 \varepsilon_{Si} \cdot N_{sub}}} \cdot \exp\left(\frac{V_{gate} - \phi_s - Q_{dep}/C_{ox} - 2 \cdot \left(V_{gate} - V_{th} - V_{off}\right)}{2 \cdot \eta \cdot \phi_t}\right)} \quad (17)$$

Then, the inversion charge density is: $Q_{inv} = C_{ox} \cdot V_{gsteff}$.

To account for the influence of V_{ds}, the channel carrier density is given by[1]:

$$Q_{ch(y)} = Q_{inv} \cdot \left[1 - \frac{A_{bulk} \cdot V_{F(y)}}{V_{gsteff} + 2\phi_t}\right] \quad (18)$$

where $V_{F(y)}$ is quasi-Fermi potential at the given point of y, along the channel with respect to the source. A_{bulk} accounts for the bulk charge effect and is simply adopted as [8]:

$$A_{bulk} = 1 + \frac{\gamma}{2 \cdot \sqrt{\phi_{s0}}} \quad (19)$$

where $\gamma = \sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot N_{sub}} / C_{ox}$ is body coefficient.

Based on the charge voltage model, the drain current expression as function of gate and drain voltage is developed. Effects including gate poly-silicon depletion effect, channel length modulation (CLM), drain induced barrier lowering (DIBL) and the mobility degradation due to high electric field as well as velocity saturation are included.

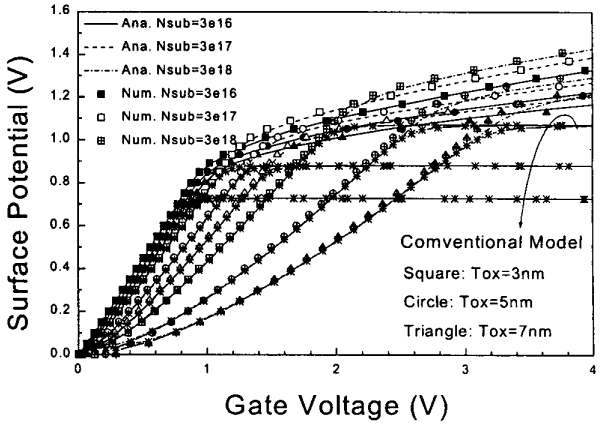

Fig.3: Surface potential of inversion layer in MOS structure with respect to gate voltage. Conventional model results are shown by lines with asterisks.

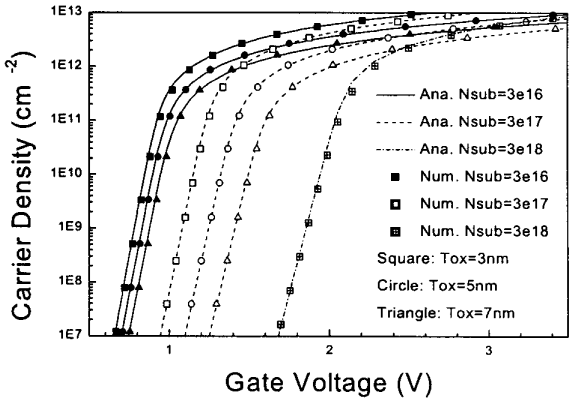

Fig.4: Inversion layer carrier density in MOS structure with respect to gate voltage.

3. Model Results and Discussions

The calculated surface potentials of the present model are shown in Fig.3 together with numerical results. For comparison, results of conventional model without consideration of inversion layer thickness and depletion charge increase after strong inversion are also shown in the figure by lines with asterisks on them. It is clearly shown that in the large range of substrate doping levels and gate oxide thickness, the model results are satisfactorily coincident with numerical results. It is also shown that even if the threshold

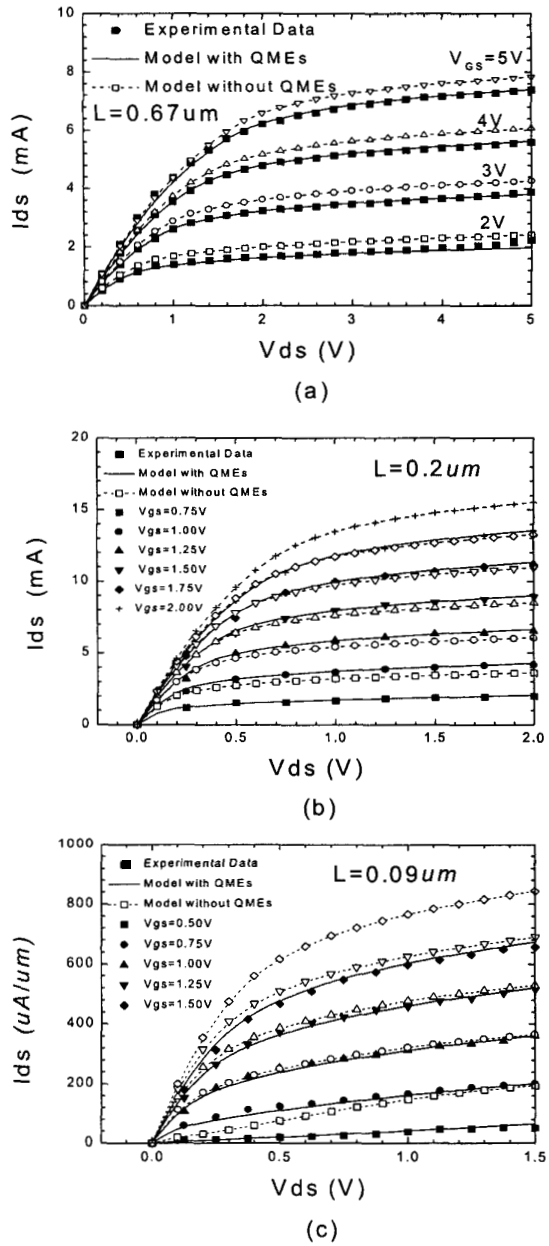

Fig.5: Output characteristics of sub-micron and deep sub-micron meter MOSFET's with different gate lengths.

voltage shift is included, the conventional model has significant errors in strong inversion region.

Inversion carrier sheet densities are shown in Fig.4. The meaning of symbols and lines are same as that in Fig.3. The high accuracy as well as the smooth transition characteristics of the model is demonstrated in the figures.

The current voltage characteristics are given in Fig.5. Output characteristics of devices with different gate lengths and different technologies are used to demonstrate the feasibility of the model. The results without considering QMEs are also shown in the figures. It is shown that models without consideration of QMEs give out much higher drain currents with respect to experimental results. The differences are larger for smaller transistors.

4. Conclusions

The concept of Space Charge Capacitance (SCC) is used to build up a new analytical charge model of quantized inversion layer in MOS structure together with the drain current model. Model results are compared with both numerical results of carrier sheet density and surface potential in the channel and experimental results of I-V data for sub-micron and deep sub-micron MOSFET's down to 0.09 μm effective gate length and the accuracy of the model is demonstrated. It is concluded from the work that QMEs have substantial influences on drain current and must be included in analytical I-V models.

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