A simulation system for capacitance variation by CMP process including defocus effect

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Abstract

We have developed a total interconnect simulation system including a CMP model. The capacitance variation due to pattern width difference by defocus effects on a globally non-uniform surface by CMP is simulated with this system. It is also shown the way to reduce the capacitance variation by CMP process derived with these simulations.

1.Introduction

Logic LSIs are developed to realize the system-on-chip(SOC). For the purpose, the reduction of not only wiring delay but also cross-talk noise has become one of the essential problems. Many interconnect models have been developed using such as the hierarchy modeling, parameter extraction with table looked up method and transmission line model[1], which can calculate the parasitic parameters within 10% errors. But, these models neglected the process parameter variation dependent on the backend process, which has become important to reduce the calculation errors. One of the most evident variation is CMP global thickness distribution in a chip. Some models[2] are developed and discussed the capacitance variation by CMP process using statistical method. In these discussions, however, pattern width difference by the defocus effects has been left out of consideration, which can have negligible effects on the capacitance. So we have developed a simulation system, and for the first time we have simulated the capacitance variation owing to defocus effects on a non-uniform surface, and discussed the impact on LSI design.

2. Model and Systems

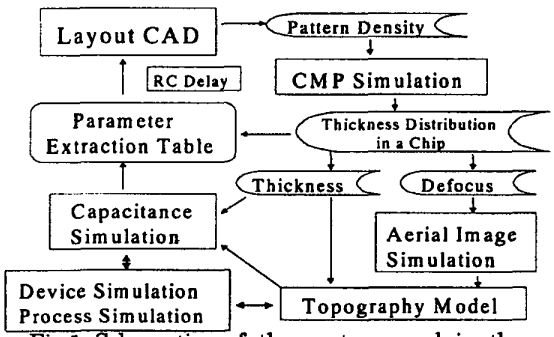

Fig.1 Schematics of the system used in these simulations.

Fig.1 shows the schematic view of the proposed simulation system realized on the ENEXSS 3D process and device simulation subsystem of Selete[3]. We have (1)developed the CMP model[4] as to calculate the long-range oxide film thickness distribution of multi-layer metal process, and "pluged-in" into the system, (2)modified the fast aerial image simulation module for accurate profiles taking the acid diffusion and photo-resist thickness effect into accounts by the convolution of photo-intensity and Gaussian, and(3)developed a parameter extraction table and interface modules to calculate the interconnect characteristics for the application to LSI design. In this work we utilized a 3D topography simulator using the equiv-contour method and calculating etching and deposition profiles based on the simulated photo-image, a 3D capacitance simulator using control volume method, a mesh generator, a 3D graphic viewer, and a framework to control the system. This system is also applied to the precise capacitance simulation, for the purpose, these module is operated with the common language(scl) of our system.

The practical simulation procedures are as follows. The relation between defocus and line width is calculated with the contour line of 1D aerial images convoluted by Gausian. Then the wire 3D topography is simulated with the process simulator. Capacitance between wires is calculated with the 3D device simulator and tabled with oxide thickness and line width. Then the oxide film thickness distribution is calculated with the CMP model. Capacitance variation in a Chip is extracted from the look-up table using the oxide film thickness and line width.

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3.Results and Discussions

In the previous work[4], it is shown the simulated results of oxide film thickness difference with CMP are agree with experiments within 5% errors as shown in Fig.2, and the long-range thickness difference using the test pattern is about 0.7 μm.

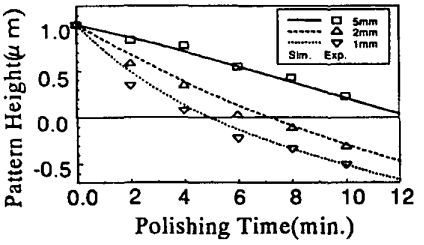

Fig.2 The results of our previous works[4]. CMP simulation agree with the experiments within 5% errors.

We investigated the influence of thickness difference with CMP including the defocus effect on the capacitance variation. First for the KrF optics(NA=0.6, σ=0.5, diffusion length of Gausian correlation is 0.1 μm), the relation between the simulated line width and defocus is shown in Fig.3. The line width change with CMP is found 3% in the defocus range of ±0.35 μm(just central focus), but line width change rapidly with defocus increase. It is also found that if the defocus is larger than 0.9 μm, 0.3 μm L&S patterns are non-resolved, so focus margin is less than 0.9 μm.

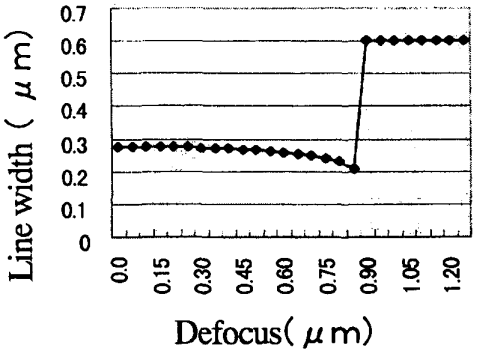

Fig.3 Line width change by defocus is shown as the result of the lithography simulation.

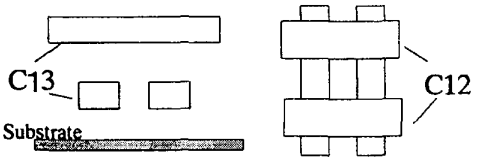

Fig.4 Schematics for wire geometry used in the simulation. The parallel capacitance(C12) is calculated.

Then we have investigated capacitance variation. It is found that when wire width becomes narrower, the total wire capacitance decreases but wire resistance increases. Considering these trade-off relations, RC delay is thought almost constant. So we investigate the parallel capacitance which causes backward cross-talk. The wire geometry used in the simulation is schematized in Fig.4, parallel capacitance(C12) between wires in 2nd metal layer is examined in the calculation. Cross capacitance(C13) is found less effective to defocus. The relation of capacitance to the oxide layer thickness calculated with and without the consideration of defocus effect are shown in Fig.5. In the simulation of the 2nd metal layer lithography, defocus is set to 0, when the oxide thickness is 0.6 μm and focal point changed together with the thickness. It is found that if the oxide thickness is larger than 1 μm, capacitance variation by the defocus effect becomes larger and more than 10% when oxide thickness is 1.2 μm.

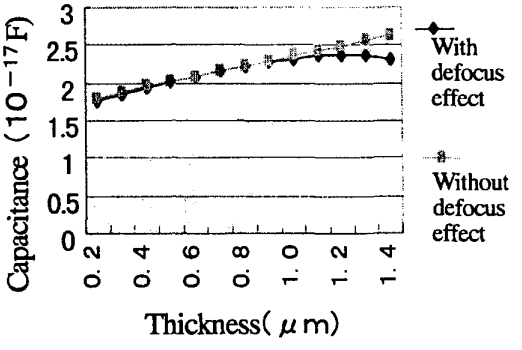

Fig.5 The capacitance between parallel metal wires vs. internal oxide thickness. The effects of defocus on capacitance is also examined.

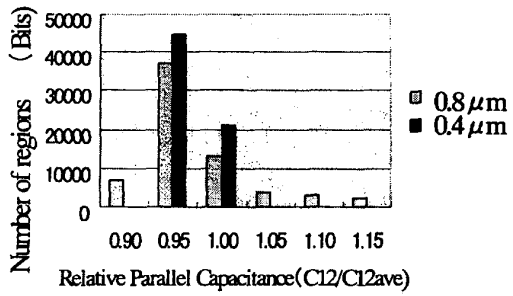

Fig.6 A histogram of numbers of the regions for parallel capacitance. Capacitance variation is reduced by 17% by the defocus.

Fig.6 shows the histogram of capacitance for parallel wires (C12) of the geometry in Fig. 3 derived from the total interconnect simulation including CMP model. In Fig.6 parameters are focus points, one is at the top of the oxide layer with thickness distribution by CMP process(focal point is just on the photo-resist when oxide thickness is 0.8 μ m) and the other is the bottom of oxide layer (focus is justified when oxide layer is 0.4 μ m). Capacitance variation ((Cmax-Cmin)/Cave) in a chip is 26% at the top(0.8 μ m) and 9% at the bottom(0.4 μ m). It is remarked that about 17% of capacitance variation by CMP process can be reduced by the focus position. We think this is one of the effects of these simulations. Fig.7 shows the capacitance distribution in a chip simulated with CMP model including defocus effect.

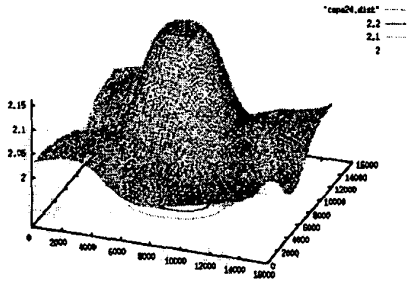

Fig.7 Capacitance distribution in a chip by CMP process including defocus effects

Then we calculated the dependence of the difference of capacitance variation by CMP process at the top focus and at the bottom on the coherency(σ). The result is shown in Table1. It is found the capacitance variation is reduced with high coherency. If the coherency is 0.8 the difference of capacitance variation is 6 % , which is less than 40% of that with coherency of 0.5. Optical parameters to reduce the parallel capacitance variation are found to be optimized with this system. Therefore this system is useful to reduce cross-talk.

σ	Upper focus (0.8 μ m)	Lower focus (0.4 μ m)	Differece (%)
0.5	26.0	9.2	16.8
0.7	29.9	15.1	14.8
0.8	26.1	20.0	6.0

Table1 Capacitance variation dependence of focus and coherency is tabled.

With this system also include the precise 3D topography and capacitance simulation modules. An example of precise 3D topography simulation is shown in Fig.8. Wire rounding by light interference is reproduced. These precise simulation results are incorporated into the look-up table and applied to LSI design.

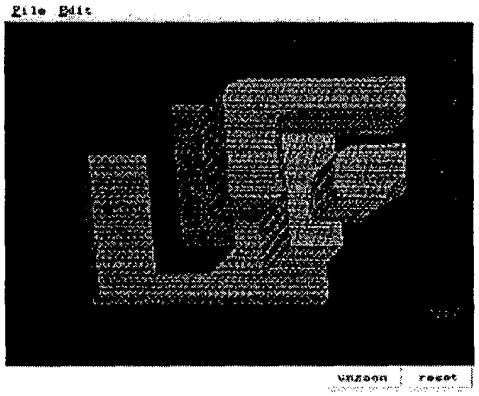

Fig.8 A result of precise 3D topography simulation. With this topography 3D capacitance is simulated.

4. Conclusion

"The capacitance variation due to defocus effects on a globally non-uniform surface by CMP" is simulated for the first time. With this model, with the defocus adjustment, capacitance variation by CMP process can be reduced. These models are useful for interconnect design.

5.Acknowlegements

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