An Exhaustive Method for Characterizing the Interconnect Capacitance Considering the Floating Dummy-Fills by Employing an Efficient Field Solving Algorithm

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Abstract - **This paper presents an exhaustive method to characterize the interconnect capacitances with taking the floating dummy-fills into account. Results of the case study with typical floating dummy-fills show that the inter-layer capacitances are also an important factor in the electrical consideration for the dummy-fills. An efficient field solving algorithm is implemented into the 3D finite-difference solver and its computational efficiency is compared with the industry-standard RAPHAEL. Furthermore, the overall flow for extracting the parasitic capacitance considering the dummy-fills at the full-chip level is discussed and the underlying assumption is testified.**

I. INTRODUCTION

The insertion of dummy metals contributes to reduce the pattern-dependent variations of the dielectric thickness in the CMP process[1], as shown in Fig. 1, since the dielectric thickness strongly depends on the pattern density of the underlying metal layer. However, such dummy-fills change the electrical characteristics of interconnects, such as signal delay or crosstalk, significantly[2]. It acts in quite different ways depending on whether it is grounded or on the floating state. As explained in Fig. 2 and Table I, the coupling capacitance is increased by the floating dummy; thus, the new crosstalk path is formed. On the contrary, the signal delay becomes worse with the grounded one. With the floating dummy-fills, which is preferred for ASIC designs due to the short design time and considerable area to be filled, the electrical characterization is a formidable task. The current parasitic extraction tools do not handle the floating dummy-fills well and the field solvers are not optimized for them. In this study, a new methodology and computational algorithm to treat the floating dummy-fills in characterizing the interconnect capacitances are proposed.

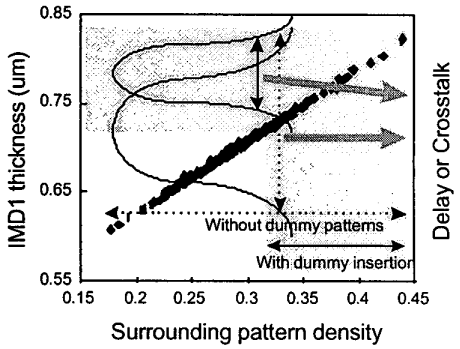

Fig. 1. IMD thickness versus pattern density of a 0.25um logic process. The IMD thickness is calculated using CHAMPS[3], an in-house CMP simulator.

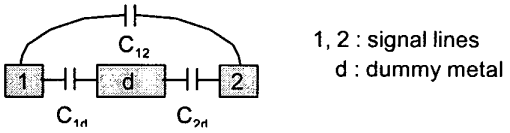

Fig. 2. A simple structure including a dummy-fill and its capacitance components. This structure is symmetric.

TABLE I
THE COMPARISON OF THE CAPACITANCE COMONENTS BETWEEN GROUNDED AND FLOATING DUMMY-FILL CASES

	Grounded		Floating
Coupling Cap. between 1 & 2	C_{12}	<<	$C_{12} + C_{1d}*C_{2d} / (C_{1d}+C_{2d})$ $\approx C_{1d} / 2$
Total Cap. of 1	$C_{12} + C_{1d}$ $\approx C_{1d}$	>	$C_{12} + C_{1d} * C_{2d} / (C_{1d}+C_{2d})$ $\approx C_{1d} / 2$

II. EFFECT OF DUMMY-FILLS ON INTERCONNECT CAPACITANCES

Fig. 3 shows a typical example of the floating dummy-fills. Such dot array in the oblique alignment is often adopted for minimizing changes in the coupling capacitances and maximizing the uniformity of the pattern density. In Fig. 4, simulation results for the capacitances are plotted. The overlap capacitance in the figure is a sum of pure area ($\varepsilon A/d$) and the fringing components. Changes in the coupling capacitances decrease, while those in fringe components increase as the space becomes larger. Due to such different trends, changes in the total capacitance of about 16% remain unchanged. The floating dummy fill results in the indirect coupling between

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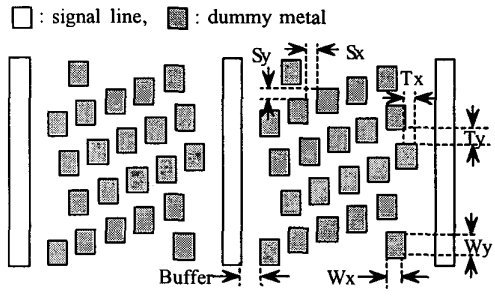

Fig. 3. The floating dummy-fills of the dot-array type (Top view).

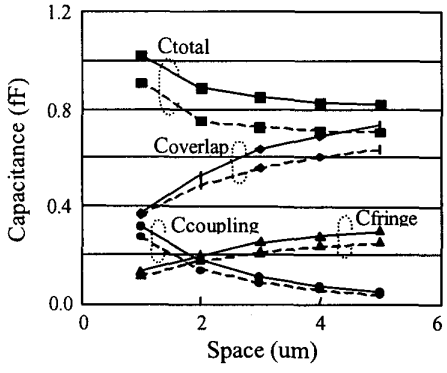

Fig. 4. Interconnect capacitances for the structure in Fig. 3. Results are obtained using the 3D field solver PASCAL. Solid and dotted lines are capacitances with and without dummy-fills, respectively. The metal plane is placed at the bottom of the structure. Signal lines are 0.5um x 6um. Wx = 0.5um, Wy = 0.5um, Sx = 0.25um, Sy = 0.25um, Tx = 0.25um, Ty = 0.5um, and Buffer = 0.25um.

the signal line and the bottom layer. This result indicates that the inter-layer capacitances are important factors in the electrical consideration for the dummy-fills.

III. Efficient Field Solving with Floating Electrodes

For the electrical characterization or optimization of design rules for the dummy-fills, a huge number of simulations are required for structures such as one in Fig. 3. However, the existing field solvers, such as RAPHAEL[4], are not optimized for the capacitance calculation with floating electrodes as shown in Table II. In the previous methods, the floating electrode is treated as a normal electrode, being imposed by the Dirichlet boundary condition, as shown in Fig. 5(a). In addition, a full circuit including floating nodes is constructed or an outer nonlinear iteration is introduced.

TABLE II

The comparison of the calculation time between RAPHAEL and PASCAL. Simulation is performed on HP C3000. Permittivity is set to be 1000 in the approximation.

Space (um)		1	2	3	4	5
# of dummy metals		5	24	42	60	78
CPU time (sec)	RAPHAEL	22	506	1768	4483	6960
	PASCAL	**2**	**9**	**14**	**21**	**24**
	PASCAL (approx. with dielectric)	5	29	71	102	138

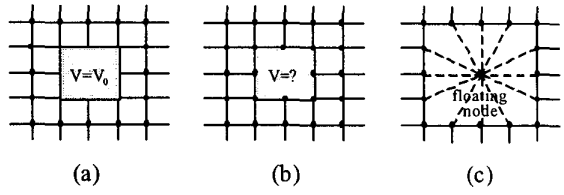

Fig. 5. Meshes with (a) Dirichlet condition on surface of the floating electrode, (b) present method, and (c) present method with node merging. Filled circles denote the nodes at which the Laplace's equation is solved.

In the present method, on the contrary, the boundary condition is not imposed and the Laplace's equation is directly solved on the surface of the floating electrode, as shown in Fig. 5 (b) and (c). To treat the equi-potential condition on the surface of the floating electrode, surface nodes are merged into the floating node.

Laplace's equations at N nodes including n floating nodes are expressed as one linear matrix equation, $A \cdot \phi = b$, where

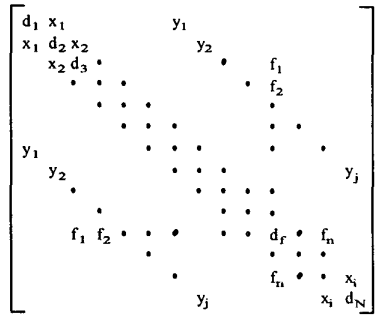

Fig. 6. The structure of the sparse matrix A in the linear matrix equation $A \cdot \phi = b$. Diagonal elements d_i are the sum of couplings with neighboring nodes. Two bands, x_i and y_i, are from the couplings in x- and y-directions, respectively. The couplings between the floating node and its neighboring nodes are contained in elements f_i.

$A \in R^{NxN}$ is a sparse matrix, $\phi \in R^N$ is a potential vector. While the matrix A has five (seven) rough bands and zero elements between bands for the 2-D (3-D) finite difference mesh and the normal Dirichlet condition, it has additional non-zero elements in rows and columns related to floating nodes in the present method as shown in Fig. 6. The capacitance obtained by solving the above linear equation contains the indirect coupling effect via the floating conductors. Thus, the effective capacitance matrix for active conductors is evaluated without constructing the full bare capacitance matrix and without nonlinear iteration such as the Newton method. It is computationally efficient and no major modifications to existing codes are required.

The present method is implemented to PASCAL, an in-house 3D finite-difference (FDM) solver. It has similar features with those of RAPHAEL, including the automatic adaptive meshing. With the proposed algorithm, the calculation times are significantly reduced compared to those of RAPHAEL, as given in Table II. The calculation time does not increase drastically as the number of floating electrodes increases. The floating electrode may be modeled with the dielectric of high permittivity. However, results in Table II show that the present method is much more efficient than such an approximate approach with dielectric.

IV. Capacitance Database Generation Considering Dummy-Fills

There are several difficulties in extraction and characterization of interconnect capacitances in the full-chip scale when dummy-fills are in floating. As mentioned, the modern parasitic extraction tools have problems in dealing with the floating capacitances. In addition, the dummy patterns do not exist in the layout at the parasitic extraction step. To circumvent these problems, the effects of the floating dummy-fills are considered in building the capacitance database for generic structures[5][6]. With this database, the rule-deck for the parasitic extraction tool is generated. Then, the parasitic extraction is performed with the layout that contains no dummy patterns. Fig. 7 describes an overall characterization flow with taking the dummy-fills into account. This flow is implemented into *S-ICE* (Samsung Interconnect Characterization Environment).

The proposed flow is based on the assumption that the capacitances are insensitive to the relative positions between dummy patterns in different layers. To testify that assumption, simulations for the structure in Fig. 8 are performed. As shown in Table III, the intra-layer (S3A-S3B) and the inter-layer(S2-S3A) capacitances vary by less than 2% as the offset is changed. This result demonstrates that the explicit position of dummy patterns in neighboring layers is not an important factor. Furthermore, for the computational efficiency, dummy patterns in the middle layer between the sig-

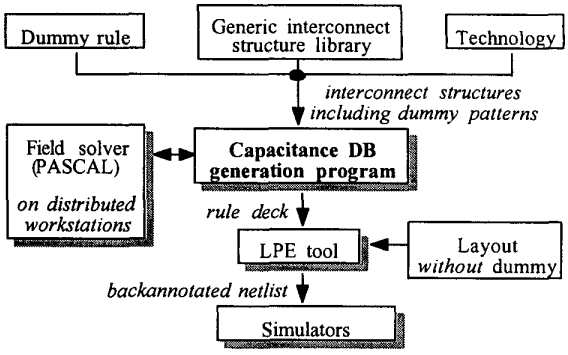

Fig. 7. The overall flow for characterizing the interconnect capacitance considering the floating dummy-fills.

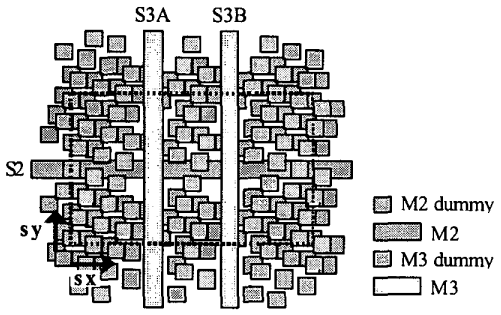

Fig. 8. A structure to testify the basic assumption. The dummy insertion rule is the same as given in Fig. 4. In simulation, the M3 layer is shifted by (sx,sy). Dotted line denotes the simulation window. The metal plane is placed at the bottom of the structure.

TABLE III
CALCULATED CAPACITANCES FOR THE STRUCTURE IN Fig. 8.

sx (um)	0	1	2	0	0	2
sy (um)	0	0	0	1	2	2
C(S3A-S3B) (fF)	0.206	0.206	0.206	0.202	0.202	0.202
C(S3A-S2) (fF)	0.252	0.252	0.253	0.250	0.250	0.252

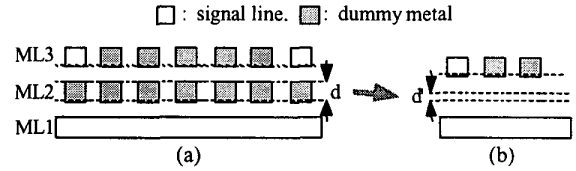

Fig. 9. Approximation of a dummy metal layer (Side view). (a) A real structure. (b) An approximated structure. d' = d * (1 - P), P is determined by the dummy pattern density.

nal and the bottom metal plane are approximated by reducing the dielectric thickness as plotted in Fig. 9. Validity of this approximation was proven in the case study performed by Kahng[7].

V. CONCLUSIONS

The electrical effects of the floating dummy-fills in interconnect structures are discussed and a new interconnect capacitance characterization methodology considering dummy-fills at the full chip level is presented. Furthermore, a robust field solving algorithm, which is especially efficient for the interconnect structures containing dummy-fills, is also proposed and its computational efficiency is verified.

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