Sub-Continuum Thermal Simulations of Deep Sub-Micron Devices under ESD Conditions

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Abstract-**The decreasing dimensions of IC devices is rendering the heat diffusion equation highly inaccurate for simulations of electrostatic discharge (ESD) phenomena. As dimensions of the heated region in the device are reduced far below 200 nm, neglecting the ballistic, sub-continuum nature of phonon conduction in the silicon lattice can strongly underpredict the temperature rise. This work integrates the phonon Boltzmann Transport Equation (BTE) in deep sub-micron silicon devices and presents a general methodology for solving the BTE. The approach developed is applicable to both Si and SOI devices and predicts temperature rises consistent with failure voltage measurements for practical devices.**

I. INTRODUCTION

Scaling of integrated circuits has reduced the characteristic length scales of the device (180 nm) and the heat deposition region corresponding to electron-optical phonon scattering (10 nm) below the mean free path of the phonon-phonon collisions, which transport heat out of the device. The phonon-phonon mean free path is approximately 300 nm at room temperature and 35 nm near the melting point of silicon [1,2]. Consequently, the continuum approach of the heat diffusion equation is no longer valid, and the distribution of phonon energy carriers must be calculated using the Boltzmann Transport Equation (BTE) in order to obtain more accurate temperature distributions [1,2]. The major discrepancy between the two modeling approaches is caused by the small heat source effect schematically illustrated in Fig. 1 [2]. When the heat source is smaller than the mean free path, Λ, of phonon-phonon collisions, a reduced number of collisions in the near heat source region result in a non-equilibrium situation within the phonon system. Heat is not removed efficiently because hot energy carriers in the heat source do not interact with the cool energy carriers in the bulk. Conventional heat diffusion theory does not capture this sub-continuum or nonlocal effect, which can be simulated using the BTE. An analogy can be found in device simulation where conventional drift-diffusion theory cannot capture effects such as velocity overshoot and nonlocal impact ionization, which are caused by the fact that the electron energy distribution cannot follow the electric field as the latter changes appreciably within a few electron mean free paths [3,4].

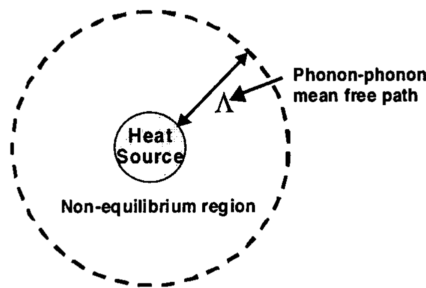

Fig. 1 Schematic of non-equilibrium small heat source effect.

These sub-continuum effects are particularly important for short transient high-current events such as electrostatic discharge (ESD). ESD is a major cause of IC failures [5]. Each new generation of IC technology requires new ESD protection designs, which are optimized through extensive experimentation [5]. Accurate ESD modeling techniques can help minimize the design time for protection circuits. However, existing thermal modeling based on heat diffusion theory is unable to accurately predict ESD failure without fitting adjustable parameters to experimental data [5]. Previous work has primarily focused on DC (steady state) electrical and thermal simulation [6] which does not represent an ESD event and can lead to predictions of temperatures approaching failure levels at sub-critical currents because of higher self-heating and thermal impedance. In addition, existing circuit simulators use analytical heat diffusion techniques, which require the use of constant thermal properties. These properties are typically evaluated at the second breakdown temperature (600-1000 °C) [7], resulting in lower values of the thermal conductivity throughout the simulation domain and in artificially high predicted temperatures. This work combines a new transient heat transport modeling approach with electrical simulation to create a new simulation methodology for predicting the temperature fields in transistors during ESD events. This is the first step towards enabling a circuit simulator such as SPICE to accurately simulate transient high current phenomena for predicting ESD failures.

II. SUB-CONTINUUM (BTE) THERMAL SIMULATIONS

The BTE describes the rate of change of the phonon carrier distribution through motion, scattering, and generation of phonon energy carriers. The transient BTE can be expressed in terms of the distribution of phonon energy per

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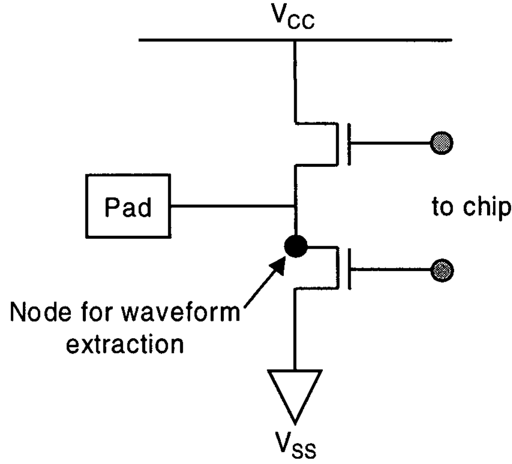

Fig. 2 ESD protection circuit used in this study.

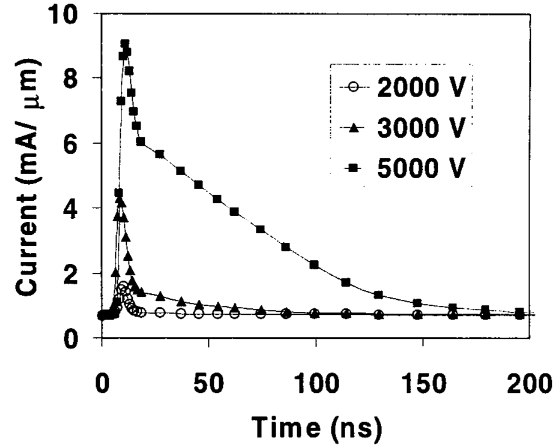

Fig. 3 ESD waveforms from circuit simulations.

unit volume per unit solid angle and can be expressed in the relaxation time approximation as:

$$\frac{\partial e''}{\partial t} = -v \cdot \nabla e'' + \frac{e''_{eq} - e''}{\tau_{phonon}} + q_{electron-phonon} \quad (1)$$

where e'' is the phonon energy per unit volume, per unit solid angle. In these simulations, the phonon velocity is assumed to be isotropic and is given by v. The second term on the right of (1) accounts for phonon scattering in the relaxation time approximation using the equilibrium energy density, e_{eq}'', and the phonon scattering rate, τ_{phonon}. The phonon scattering rate is calculated from the phonon mean free path, $\Lambda = v\tau_{phonon}$, which is extracted from the silicon thermal conductivity using the kinetic theory expression:

$$\Lambda = \frac{3k}{Cv} \quad (2)$$

where k is the thermal conductivity and C is the heat capacity per unit volume. The temperature dependence of k and C are accounted for in the model. Optical phonon energy absorption from highly energetic or hot electrons is considered using the source term $q_{electron\text{-}phonon}$. The scattering rate between electrons and optical phonons is approximately two orders of magnitude faster than the phonon-phonon collisions responsible for heat transport [8]; consequently, the energy transfer mechanism between electrons and phonons is taken to be instantaneous. Electrical device simulation is used to calculate the time dependent heat generation in the transistor and is used as the $q_{electron\text{-}phonon}$ input parameter in (1). Equation (1) is discretized and integrated forward in time using implicit time stepping techniques, and the temperature distribution is extracted from the phonon energy distribution using:

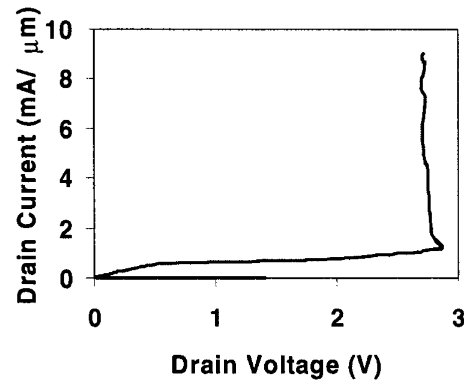

Fig. 4 High current transient I-V curve generated for a 5000 V HBM ESD event using a device simulator.

$$e'' = \int C dT \quad (3)$$

III. ELECTRICAL SIMULATIONS

The Human Body Model (HBM) is the most widely used model for an ESD event. In this work, realistic current waveforms at the NMOS protection transistor in an ESD circuit (shown in Fig. 2) [9] are calculated using a circuit simulator. These transient waveforms (Fig. 3), corresponding to HBM voltage levels of 1000 V, 2000 V, 3000 V, and 5000 V applied to the external I/O pins, are imported into a device simulator as a current boundary condition on the NMOS. The device simulator generates the high current I-V characteristics as shown in Fig. 4. The time-dependent heat generation profile is extracted for subsequent thermal simulations, which are not coupled to the electrical simulators. Both the circuit and device simulations are performed at room temperature to provide the worst case

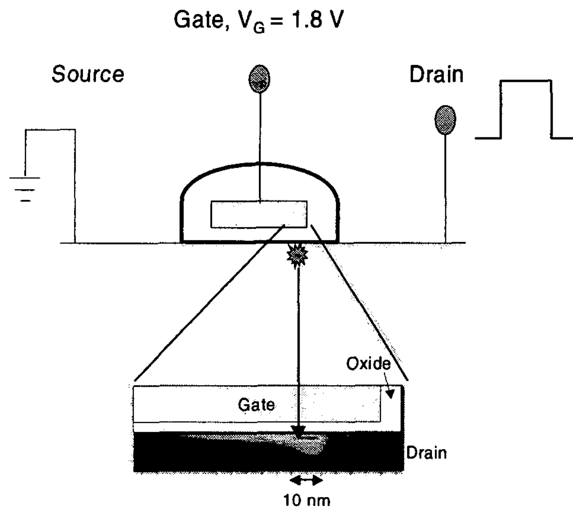

Fig. 5 Schematic and simulated (blown up region) transistor heat generation profile.

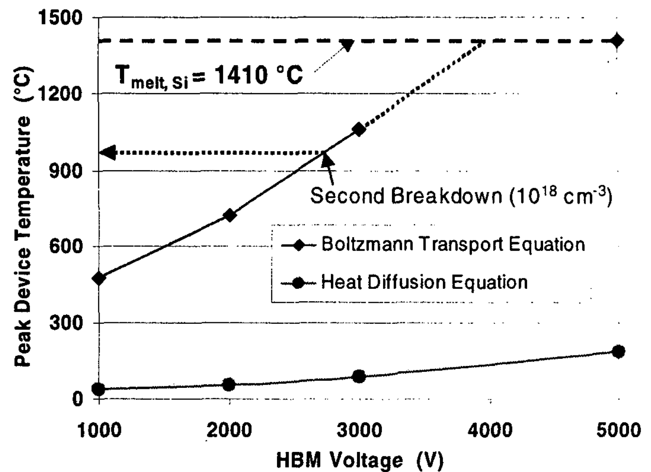

Fig. 6 Comparison between peak transient device temperatures obtained using the Boltzmann transport equation and standard heat diffusion equation under various ESD stress conditions.

scenario because the current and heat generation will decrease with increasing temperature. The interaction between electrons and phonons results in a heat generation region with characteristic length scales on the order of 10 nm as seen in Fig. 5.

A. Isolated NMOS Transistor Simulations

Before combining ESD protection circuit simulations with electrical and thermal device simulations, the simpler case of a single isolated transistor was characterized. Sub-0.35 μm NMOS breakdown I-V characteristics were experimentally measured by stepping the drain current from 0 to 5 mA/μm with one hundred 0.05 mA/μm steps of 640 μs duration. After the 640 μs current pulse at the peak current of 5 mA/μm, the device failed. Failure analysis revealed that a filament developed between the source and drain region while the gate oxide remained intact, indicating a thermal failure.

First, the standard diffusion (continuum) model is applied to predict the failure temperature. A worst case approximation is made in which the stress current is assumed to be constant at 5 mA/μm. The transient thermal simulation is taken to steady state. Under these conditions the device is expected to fail, considering the fact that it failed with much lower input power in the actual experiment. The peak steady state temperature from the transient heat diffusion equation is 455 °C, which is about 550 °C less than the estimated temperature (1000 °C) required for second breakdown (and eventual thermal runaway) at a doping level of 10^{18} cm^{-3} [5].

A second set of simulations is performed using the BTE in order to compare the two modeling approaches. The temperature from the BTE simulations exceeds the melting point of the silicon substrate before the steady state is reached, and the temperature across the entire channel region of the device is elevated to greater than 530 °C. This indicates that the diffusion equation does not predict a thermal melting failure even for the worst case assumption of a constant 0.5 mA/μm current, while the BTE calculation explains the thermal failure mechanism of the device.

B. ESD Protection Circuit Simulations

As stated in the electrical simulation section, a circuit simulator is used to generate ESD current waveforms for 1000 V, 2000 V, 3000 V, and 5000 V HBM input voltages. The peak temperature results are plotted in Fig. 6 for the BTE and the heat diffusion simulations. It can be observed that the diffusion equation results in peak temperatures that remain below 300 °C for all HBM voltages. This is significantly lower than the temperature required for second breakdown and eventual thermal runaway [5]. In the BTE simulations, the non-equilibrium situation caused by the small heat source dimension causes the temperature rise to increase dramatically. For the 5000 V HBM case, the simulation was stopped when the temperature reached the melting point of silicon. The trend in the device temperature obtained using the BTE for HBM voltages varying from 1000 V – 3000 V is expected to continue as shown by the dashed line. These simulations are useful because they demonstrate that under short current transients, the BTE temperature rise greatly exceeds the diffusion results and can explain device thermal failure. This new thermal model is expected to improve the accuracy of circuit level ESD simulations.

IV. SUMMARY AND CONCLUSIONS

In this paper, sub-continuum thermal simulations are performed on sub-0.35 μm NMOS devices to obtain the peak temperature rise under transient high current (ESD) conditions. Temperature predictions using this approach are compared with those from the classical heat diffusion theory, which is presently used in all device and circuit simulators. This work demonstrates that the new thermal simulation approach, which accurately accounts for phonon physics in the deep sub-micron regime, can better explain the thermal failures of isolated transistors. It is shown that the sub-continuum thermal model yields a significantly higher temperature rise when compared with heat diffusion modeling in ESD protection circuits. The existing heat diffusion modeling results in transistor temperatures that are not consistent with thermal failures typically observed at second breakdown. Further comparisons with experimental failure data are underway to ensure the highest level of accuracy before incorporation of these models into device and circuit simulators.

ACKNOWLEDGMENT

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