A Fast Three-Dimensional MC Simulator for Tunneling Diodes

Mathias Wagner, Hiroshi Mizuta, and Kazuo Nakazato
Hitachi Cambridge Laboratory, Hitachi Europe Ltd.
Madingley Road, Cambridge CB3 0HE, United Kingdom

Abstract–**A fast simulator is presented for 3D vertical tunneling devices with lateral confinement and gates. The tunneling current across each barrier is calculated using a combination of 3D raytracing, Monte Carlo ensemble averaging, and a multi-grid Poisson solver, until selfconsistency of the current is achieved.**

I. INTRODUCTION

In recent years new types of electronic devices such as the PLED Transistor [1–3] have started to appear which require full 3D modelling as well as a simulation of the effect of tunnel barriers. Within the framework of conventional packages the simulation of tunnel barriers is nontrivial, as the tunnel current is manifestly a quantum-mechanical effect, and as such is beyond the capabilities of standard drift-diffusion solvers. However, some attempts have been made on the basis of this simulation technology using quantum-mechanically calibrated drift-diffusion solvers [4]. More powerful techniques based on non-equilibrium Green's functions [5] or density matrices have been proposed but, although their potential is enormous, one has to realize that these techniques are too CPU demanding for the foreseeable future, when applied to 3D devices. Here we propose an alternative route suitable for laterally gated vertical tunneling devices, where the tunnel resistance dominates the electronic transport [See Fig. 1a)].

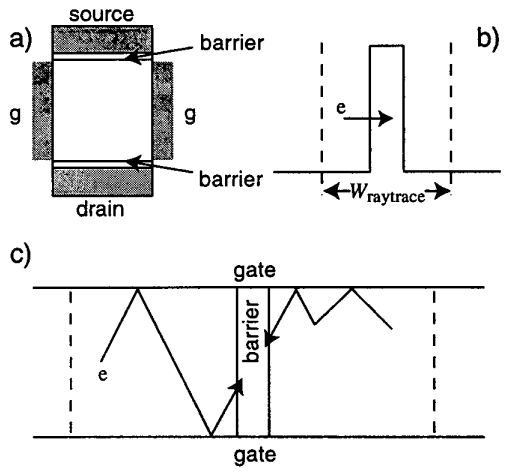

FIG. 1: a) Radial cross-section of a typical device; b) around each barrier, a ray-tracing window is defined. c) cross-section along the channel to demonstrate the ray-tracing including specular scattering. The path on the right is typical for a device under strong gate bias, where the channel has fully opened, and current flows predominantly in the vicinity of the lateral gates.

II. SIMULATOR

At the heart of our simulator is an accelerated multi-grid Poisson-equation solver [1] for rotationally symmetric vertical tunneling devices coupled to a Monte-Carlo solver to calculate the tunneling current across each barrier along the source-drain channel. The idea is that the tunnel resistance will by far dominate the current flow, leading to virtually constant chemical potentials in the regions between barriers, and all that needs to be done is to self-consistently determine the chemical potential in each region such that the tunneling current across each barrier along the current path is the same. To do this, we define an active window for each barrier [see Fig. 1b) & c)], from within which we randomly select particle positions and momenta [2]. Assuming specular lateral boundary conditions we then perform a raytracing algorithm to determine the length l of the ballistic trajectory the particle would have to cover in order to reach the barrier. The probability for the particle to actually get to the barrier is then taken to be exponentially distributed as $\exp(-l/l_c)$, where l_c is the mean-free path, which we take as a parameter (a few nm at 300 K) [3]. This weighting procedure allows us to smoothly in-

[1] The acceleration scheme used is that of modifying the Poisson equation to explicitly contain a controlling feedback term to try to predict the change in the electrostatic potential caused by changes in the charge density. This prediction is made on the basis of a finite-temperature Thomas-Fermi approximation, and allows for relaxation factors close to 100% to be used in the iteration loop to achieve self-consistency. Without such a scheme, complicated device structures tend to converge only very poorly.

[2] We have checked that the precise width of this window does not have any effect on the numerical results.

[3] The window for ray-tracing around each barrier must be chosen to be a few times larger than l_c.

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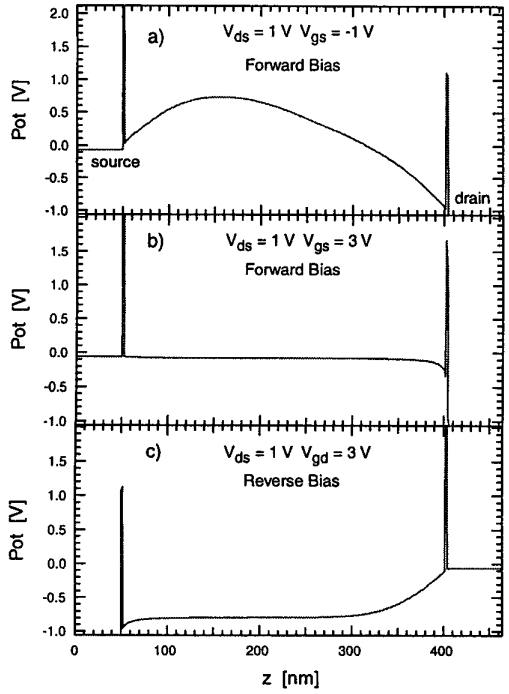

FIG. 2: Selected potential profiles at the center of the source-drain channel, $r = 0$, for various gate biases.

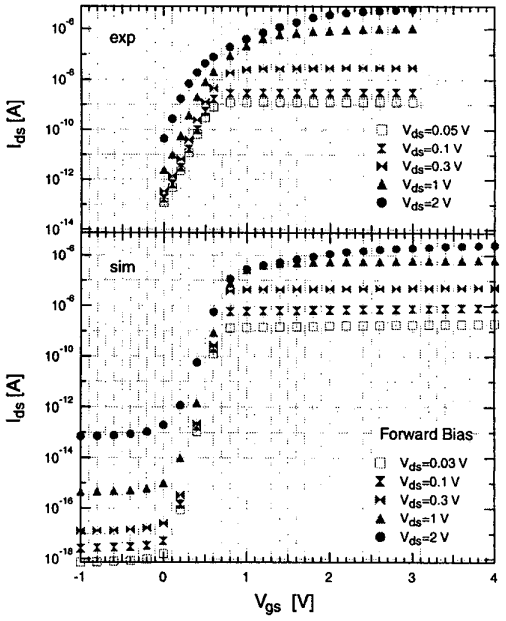

FIG. 3: I_{ds} as a function of gate bias for various V_{ds} [forward bias]. Top: experiment; bottom: simulation.

terpolate between purely coherent and incoherent transport. Eventually, the tunneling probability is calculated within the WKB approximation using the local barrier height at the point of impact. Sampling over 2-3 million particles usually gives sufficient precision.

III. RESULTS

We have studied a vertical tunneling device with a lateral nominal width of 200 nm and an intrinsic channel of 350 nm between the source and drain Si_3N_4 stopper barriers of 1.5 and 2 nm, respectively, as shown schematically in Fig. 1a). A heavily p-doped gate ($10^{20}\,cm^{-3}$) wrapped around the channel provides us with the controlling action. Source and drain contacts are n-doped ($10^{19}\,cm^{-3}$). A band diagram of the OFF state, taken at the center of the channel, is shown in Fig. 2a). At V_{gd} = -1 V the channel is completely quenched off by the action of the lateral gate [4].

Fig. 3 shows measurements (top) and simulation results (bottom) of the source-drain current I_{ds} as a function of the gate voltage for various source-drain biases, in forward bias direction, at a temperature of 300 K. The threshold characteristics measured and even the absolute values are clearly well reproduced in the simulation. The slightly sharper threshold behavior in the simulation is due to our assumption that the source-drain voltage drops over the barriers only, and thus is an indication that the channel resistance is not entirely negligible. A spatially resolved analysis of where in the channel the current actually flows shows that the largest contribution to the tunnel current in the ON state stems from the barrier region closest to the gate, as there the barrier is most heavily influenced by the electrostatic effect of the gate voltage. In reverse bias, shown in Fig. 4, the characteristics look very similar except that currents are somewhat reduced in the ON state, in particular for larger V_{ds}. This can be explained by the asymmetry in the thickness of the barriers: In forward direction, the potential in the intrinsic channel region aligns almost perfectly with the potential in the source contact [Fig. 2b)] as the source barrier is more transparent compared to the drain barrier, i.e. it poses a smaller resistance, thus causing V_{ds} to act on the drain barrier in full. In contrast, in reverse bias, such a close alignment of the potentials in the channel and the drain contact is not seen [Fig. 2c)], leading to a reduction of the ON current by about one order of magnitude for larger V_{ds}. We should like to point out that the only fit parameter used in these simulations was the thickness of the source barrier. All other parameters were taken from experiment.

Finally, in order to see whether the addition of a central barrier half-way along the channel might improve the ON/OFF ratio in the current, we have also performed simulations of

[4] We note that in order to correctly calculate the OFF current with this method one has to introduce a number of dummy barriers at the positions of the build-up of the electrostatic barriers shown in Fig. 2a), thereby effectively simulating a bias drop over this region. Usually, a few dummy barriers are quite enough, as seen in Fig. 5.

devices with a central Si_3N_4 barrier 2 nm thick. The three panels of Fig. 5 differ in the number of dummy barriers introduced to account for the central electrostatic barrier at small V_{gs}. For large V_{gs} the source-drain current is seen not depend on the number of dummy barriers. We find that the gating action is reduced at larger source-drain biases when the tunnel resistance of the central barrier becomes comparable to the gate-induced variable channel resistance. Overall, at least for small V_{ds}, we see some improvement of the ON/OFF ratio gained by introducing a central barrier.

IV. CONCLUSION

In conclusion, we have presented a new 3D simulator and applied it to various vertical tunneling transistors with lateral gate action. The agreement between measurement and simulation is excellent.

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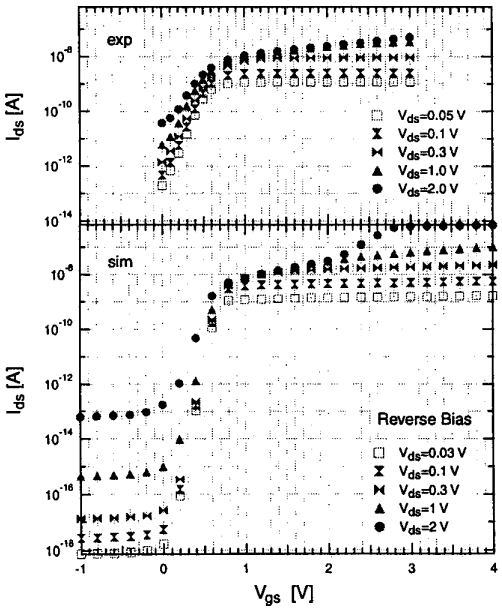

FIG. 4: I_{ds} as a function of gate bias for various V_{ds} [reverse bias]. Top: experiment; bottom: simulation.

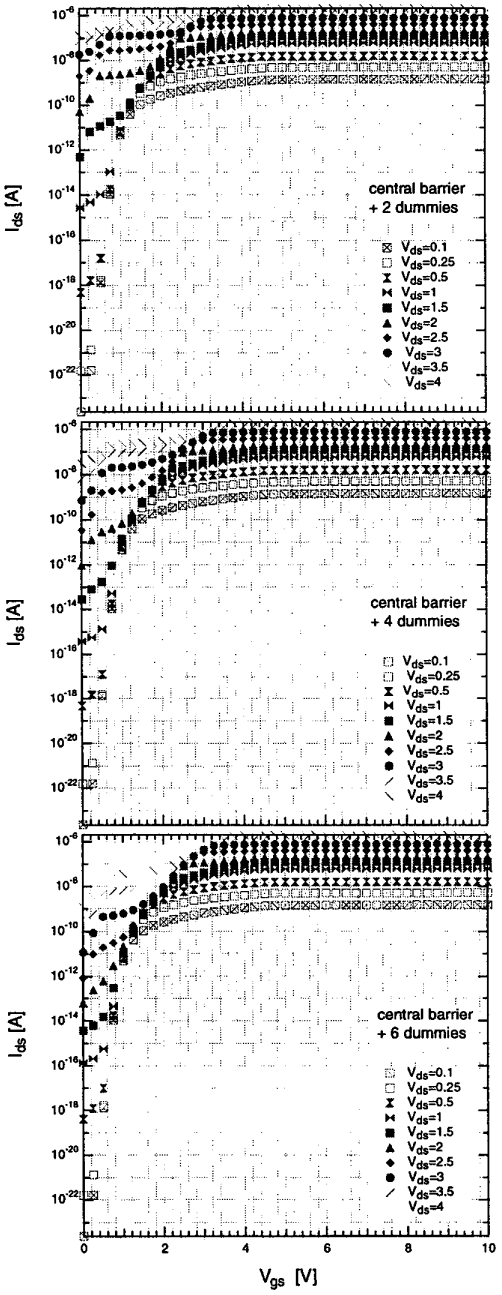

FIG. 5: Simulated I_{ds} as a function of gate bias for various V_{ds} for a device with a central 2 nm Si_3N_4 barrier. The number of dummy barriers increases from top to bottom. Their biggest effect is in the regime of small V_{gs}.