Simulation of Direct Tunneling through Stacked Gate Dielectrics by a Fully Integrated 1D-Schrödinger-Poisson Solver

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Abstract

We compare the numerical results for electron tunneling currents for single gate oxides, ON- and ONO-structures. We demonstrate that stacked dielectrics can keep the tunneling currents a few orders of magnitude lower than electrostatically equivalent single oxides. We also discuss the impact of gate material and the modeling of electron transport in silicon.

1 Introduction

Scaling the gate SiO_2 thickness below 2 nm will lead to high direct tunneling leakage currents and thus will require to use alternative materials with high ϵ like nitride, TaO_2, TiO_2, or BST. This allows to increase the physical thickness d (and thus the tunneling barrier) of the layer while keeping the same equivalent thickness d_{equiv},

$$d_{\text{equiv}} = \frac{\epsilon_{\text{Si}}}{\epsilon} d,$$

where ϵ_{Si} and ϵ are the dielectric constants of silicon and the material in question, respectively. In practice, it is also desirable to keep the excellent properties of the Si-SiO_2 interface. To combine the best of both worlds, stacked dielectrics with an oxide layer directly on the silicon substrate and a high-ϵ layer on top of it are favorable.

From a simulation point of view, the problem with stacked dielectrics is that simple WKB-based formulas for tunneling cease to work, because they rely on the assumption of a trapezoidal tunnel barrier. It is possible to generalize these models by splitting the barrier into several trapezoidal parts. However, the numerical cost increases with increasing complexity of the barrier. For complicated structures, more general approaches become more attractive as their performance disadvantage decreases.

We applied a tunneling formula based on the numerical solution of the 1D-Schrödinger equation to the problem, where all barrier shapes are admissible. We studied the tunneling currents for electrostatically equivalent oxide, ON and ONO barriers and analyzed the results.

2 Method of Computation

We start from the solutions of the 1D-Schrödinger equation

$$\left(-\frac{\partial}{\partial z}\frac{\hbar^2}{2m_z^\nu(z)}\frac{\partial}{\partial z} + V(z)\right)\psi_i^\nu = E_i^\nu \psi_i^\nu \tag{1}$$

(z-direction perpendicular to the interface), where ν labels the silicon conduction band valleys. The eigensolutions (ψ_i^ν, E_i^ν) are computed for energies from the lowest potential point in the Si up to the maximum potential in the structure. The Schrödinger equation is solved

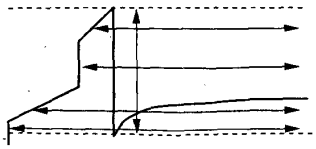

Figure 1: Band structure dependent energy range for which the Schrödinger equation is solved (vertical arrow) and Schrödinger zone as a function of energy (horizontal arrows).

for a zone that covers the entire channel and extends up to the (energy-dependent) gate-side turning point. Fig. 1 sketches energetic and spatial regions of integration.

At the end points of the Schrödinger zone we impose boundary conditions of the form $|\psi_i'^{\nu}/\psi_i^{\nu}| = \sqrt{2m_z|E_i^{\nu} - V|}/\hbar$, where the potential V and the z-component of the effective mass, m_z, are taken at the respective end points of the Schrödinger zone. These boundary conditions contain the implicit assumption that outside the Schrödinger zone V and m_z keep the values they take at its out-most point. The deviation of the actual values from these assumed values represents a perturbation for the bound states. Due to this perturbation the states decay into the gate. The decay rate is determined using Bardeen's method of the time dependent perturbation theory [1]. From this, the current density can be obtained by an integration over all states,

$$j = \frac{q\sqrt{2m_{\mathrm{g}}}L}{8\pi} \sum_{i,\nu} m_{xy}^{\nu} \int_0^{\infty} dE \, \frac{\Theta(\tilde{E} - E_{\mathrm{c,g}})}{\sqrt{\tilde{E} - E_{\mathrm{c,g}}}} \times \\ \times \left|(\psi_{\tilde{E}}/m_z)\,\partial_z\psi_i^{\nu} - (\psi_i^{\nu}/m_z)\,\partial_z\psi_{\tilde{E}}\right|^2_{z=z_0} \Delta f(E_i^{\nu} + E), \quad (2)$$

with $\tilde{E} = E_i^{\nu} + (1 - m_{xy}^{\nu}/m_{\mathrm{g}})E$. $E_{\mathrm{c,g}}$, m_{g}, and $\psi_{\tilde{E}}$ are the conduction band energy, the effective mass, and the wave function in the gate, respectively. Δf denotes the difference of the Fermi functions in gate and channel. Whereas the ψ_i are determined numerically, $\psi_{\tilde{E}}$ is obtained by a WKB type approximation involving the band edge energy in the gate, the barrier height, and the electric field at the classical turning point on the gate side of the barrier.

For 2D-structures, tunneling currents can be obtained by splitting the device in several slices perpendicular to the insulator-silicon interface. For each slice, a 1D quantum mechanical problem is solved. The total tunneling current is obtained by summing over all slices. To enable slicing of the Schrödinger zone, we use a tensor grid in this region. This allows us to take the grid lines perpendicular to the interface to solve the quantum mechanical problem on, without the need of interpolation.

While this way we are able to simulate idealized geometries where each material layer has a uniform thickness, we are not able to treat realistic devices with non-planar interfaces and laterally varying layer thicknesses [2], due to the intrinsic one-dimensionality of our approach. Since tunneling currents are very sensitive to the insulator thickness, our method is quantitatively valid only for simple test devices. For realistic MOSFETs it can only give qualitative information.

3 Simulation Results

We present results for capacitors with n^+-poly and aluminum gates, respectively, and for an n-channel MOSFET with n^+-poly gate, obtained with the device simulator DESSIS-ISE[3]. In the program, the flux of tunneling carriers (Eq. 2) across the interface between silicon and dielectric yields a local generation-recombination rate. Three different gate dielectrics are compared with each other – a 2.04 nm single SiO_2, an oxide-nitride (ON) stack with 1 nm SiO_2 and 2 nm Si_3N_4 on top, and an oxide-nitride-oxide (ONO) stack with 0.5 nm SiO_2, 2 nm Si_3N_4, and 0.5 nm SiO_2 –, all systems having an equivalent oxide thickness of 2.04 nm.

In all cases the following parameters were used: $\epsilon_{Si} = 11.7$, $\epsilon_{Ox} = 3.9$, $\epsilon_{Ni} = 7.5$, $m_{Ox} = m_{Ni} = 0.42\,m_0$, $m_{Alu} = 0.32\,m_0$, $\chi_{Si} = 4.05\,eV$, $\chi_{Ox} = 0.9\,eV$, $\chi_{Ni} = 1.9\,eV$, $\chi_{Poly} = 4.05\,eV$, $\Phi_{Alu} = 4.25\,eV$, $E_{F,Alu} = 11.7\,eV$, $E_{g,Ox} = 9\,eV$, $E_{g,Ni} = 5\,eV$. The effective masses in the poly gate were treated as in silicon. The doping concentrations were chosen as $N_D^+ = 3\times10^{20}\,cm^{-3}$ in the poly gate and $N_A^- = 5\times10^{17}\,cm^{-3}$ in silicon.

Fig. 2 shows the gate currents of the MIS capacitors with poly gate. The lines were obtained neglecting the feedback of the tunnel current on the Fermi level, whereas the symbols give the results of a fully self-consistent treatment. Both approaches give identical currents as long as the tunnel barrier is the dominant resistance in the structure. This holds for a wide range of negative and for very small positive gate voltages. For negative gate voltages the electrons are injected from the gate into the silicon. From there, they can easily flow to the back contact without encountering another barrier. Therefore, the current is mainly determined by the insulator barrier and only at very strong negative voltages limitations for the electron flux in the silicon become visible (see Fig. 3). For positive gate voltages the structure is similar to a reverse biased pn-diode. Only for very small voltages the current is determined by the insulator barrier. Even for moderate positive bias the current is limited by the generation of electrons in the depletion zone. Therefore, the full self-consistent computation of the electron transport gives currents significantly lower than those obtained with the simplified treatment. However, the results of the latter are not completely meaningless. In MISFETs, electrons can be provided via source and drain contacts. Thus, tunneling currents obtained by full self-consistent calculations of MISFETs (see Fig. 4) are similar to those obtained for MIS-diodes in the simplified treatment.

The dielectrics containing nitride suppress the current at small gate voltages by 3–4 orders of magnitude with negligible difference between ON and ONO. In Fig. 2, a shoulder at $-1.5\,V$ appears because the gate Fermi level aligns with the silicon conduction band edge. The sharp structure in the case of ONO around $-5.5\,V$ originates from the resonance when the gate Fermi level crosses the triangular-shaped ONO potential well.

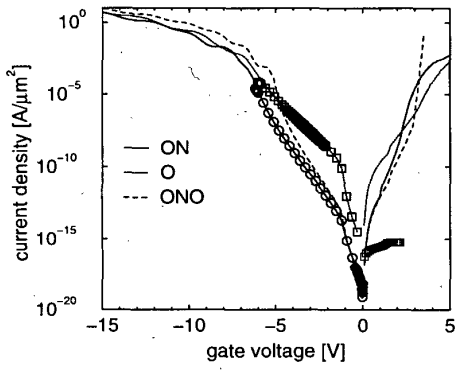

Figure 2: Simulated gate currents of MIS capacitors with poly gate containing oxide (O), oxide-nitride (ON), and oxide-nitride-oxide (ONO) dielectrics with physical thickness as indicated in the text. The lines are results for fixed quasi Fermi potential, symbols are for full self-consistent computation.

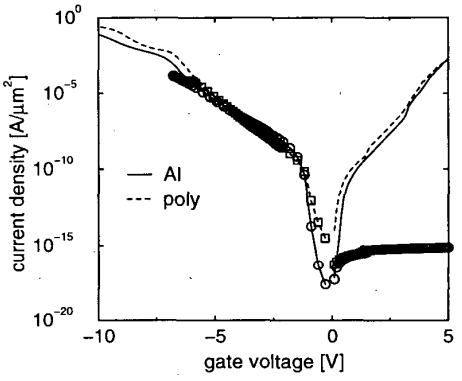

Figure 3: Simulated gate currents of MIS capacitor with single oxide dielectric. Comparison between aluminum gate and poly gate. The lines are results for fixed quasi Fermi potential, symbols are for full self-consistent computation.

The effect of the two different gate materials in the case of a single oxide is demonstrated in Fig. 3. The MOS diode with poly gate yields a larger current than the diode with aluminum gate because of the smaller work function difference, which leads to a barrier height reduction of 0.2 eV. The difference is particularly pronounced before flat-band conditions are reached. Because of the different energetic distance between gate Fermi level and silicon conduction band edge, the exponential tail of the distribution function in the gate has a large effect.

Gate and drain currents versus gate voltage at a drain bias of 1 V of an n-channel

MOSFET with 300 nm gate length, 240 nm effective channel length, 1 μm channel width, source/drain extension depths of 20 nm, and deep source/drain junction depths of 60 nm are shown in Fig. 4. The dielectrics containing nitride suppress the gate current by 3–4 orders of magnitude.

For negative gate voltage, the tunnel current in the ONO structure exceeds the current in the ON structure, whereas for positive gate voltage the situation is reversed. For moderate voltage drop, this is due to the difference in the dielectric constant of Si and nitride. As the field is stronger in the material with lower dielectric constant (SiO_2), the resistance of the overall barrier is larger, if this material is on the side of the positively biased contact. Fig. 5 illustrates this. For bigger voltage drop or high energetic electrons the conduction band of the insulators can be reached (Fowler-Nordheim regime) and this simple picture is rendered insufficient.

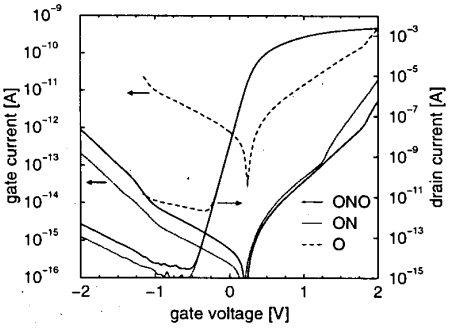

Figure 4: Gate and drain currents versus gate voltage at a drain bias of 1 V of an n-channel MOSFET with different gate dielectrics.

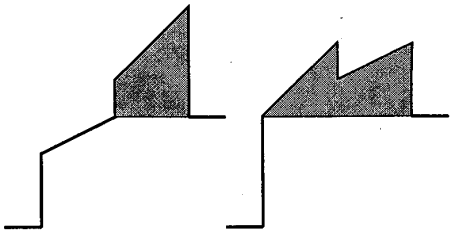

Figure 5: Conduction band edge of a ON and a NO structure at the same bias condition. The shaded area is proportional to the barrier "seen" by electrons close to the conduction band edge on the right side.

Fig. 4 shows that threshold voltage and sub-threshold swing are independent of the insulator system since the equivalent oxide thickness is the same in all cases and short-channel effects are not influenced by the very small gate thickness-to-length aspect ratio. For large negative gate bias a significant amount of the drain current is generated by tunneling electrons.

4 Summary

We have described a tunneling model based on the numerical solutions of the 1D-Schrödinger equation. This model is applicable for barriers of arbitrary shape. Embedding this model into the device simulator DESSIS_ISE enabled us to perform self-consistent and 2D calculations of device characteristics.

Comparing single oxide dielectrics to electrostatically equivalent ON- and ONO-stacks, we have demonstrated that the latter can reduce the tunneling current by several orders of magnitude. We have demonstrated that also the gate material has a significant impact on tunneling at low gate voltages.

References

[1] J. Bardeen, Phys. Rev. Letters **6**, 57 (1961).

[2] C. T. Liu *et al.*, in *1999 Symposium on VLSI Technology Digest of Technical Papers*, The Japan Society of Applied Physics (Business Center for Academic Societies Japan, 5-16-9 Honkomagome, Bunkyo-ku, Tokyo 113-8622, 1999), pp. 75–76.

[3] *DESSIS reference manual*, ISE Integrated Systems Engineering AG, 1998.