Circuit-Level Electrothermal Simulation of Electrostatic Discharge in Integrated Circuits

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Abstract
A circuit-level electrothermal simulator, MICS (MItsubishi Circuit Simulator), is presented with parasitic bipolar transistor action and lattice heating taken into account. Diffusion capacitance in parasitic bipolar transistors is introduced to cover turn-on behavior under short rise-time current. Device temperatures are simulated from calculated electrical characteristics and the closed-form solution of the heat transfer equation. Simulation results show that this tool is valuable in evaluating electrostatic discharge (ESD) robustness in integrated circuits.

1 Introduction

The destructive nature of electrostatic discharge (ESD) in integrated circuits has been becoming more apparent as semiconductor devices become smaller and more complex. The high voltages result in large electric fields and high current densities in small devices, which can lead to breakdown of insulators and thermal damage. Circuit-level electrothermal simulation[1] under ESD conditions is in great demand for reducing the time and cost necessary to establish desired reliability. The electrothermal simulation requires accurate description of the parasitic bipolar transistor action of MOSFETs, which is the relevant conduction mechanism under ESD conditions. Moreover, lattice temperature distribution must be known in order to judge ESD immunity.

In the following section, simulation models for parasitic bipolar action and lattice heating are described. These models are verified with the aid of device simulation because it is difficult to measure terminal current and voltage and temperature in a device under ESD conditions. In Section 3, simulation results for an I/O circuit are presented to show the usefulness of the proposed models.

2 Modeling

2.1 Parasitic Bipolar Transistor Action

Several elements are added to a conventional MOSFET model to express parasitic bipolar transistor action, as shown in Fig. 1. The elements, I_{ds}, I_{bs}, I_{bd}, R_s and R_d in the figure are the same as those included in conventional MOSFET models. Current sources, I_{col}, I_{base} and I_{gen} for an n-MOSFET with the gate width W are given as

$$I_{col} = W J_{0c} [\exp(V_{B'S'}/V_T) - \exp(V_{B'D'}/V_T)], \quad (1)$$

$$I_{base} = W J_{0e} [\exp(V_{B'S'}/V_T) - 1], \quad (2)$$

$$I_{gen} = (M-1)(I_{ds} + I_{coll}), \quad (3)$$

$$M = \frac{1}{1 - K_1 \exp[-K_2/(V_{D'S'} - V_{dsat})]}, \quad (4)$$

in the case of $V_{D'S'} > 0$[2]. The parameter K_2 is assumed to be the product of the exponential factor, B, of the ionization coefficient $\alpha = A\exp(-B/E)$[3], where E is the electric field strength, and the velocity saturation region length, $l_c = \sqrt{(\epsilon_{Si}/\epsilon_{SiO_2}) t_{ox} x_j}$[4]. The avalanche breakdown voltage V_{av} can be written as $K_2/\ln(K_1)$ from Eq. (4). The parameter K_1 is determined so as to fit V_{av} to measured data.

Substrate resistance, which plays a crucial role in parasitic bipolar transistor action, is defined as $R_{sub} = r_{sub}/W$.

Diffusion capacitance is defined as $C_{S\,diff} \equiv Q_{S\,diff}/V_{B'S'}$ and $C_{D\,diff} \equiv Q_{D\,diff}/V_{B'D'}$, where $Q_{S\,diff} = \tau_F I_{0c}[\exp(qV_{B'S'}/kT) - 1]$ and $Q_{D\,diff} = \tau_R I_{0c}[\exp(qV_{B'D'}/kT) - 1]$[5].

The parameters, J_{0c} and r_{sub} are determined so as to fit the I-V curve to device simulation results. The parameter, J_{0e} is set to zero because the current source, I_{base} is identical with the element, I_{bs}, which is included in the original transistor models.

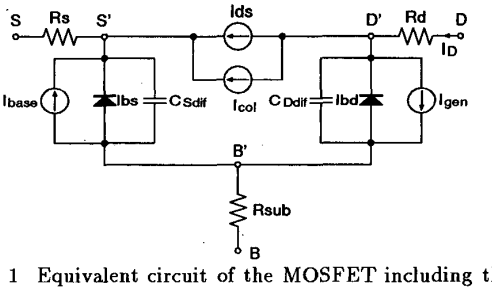

Fig. 1 Equivalent circuit of the MOSFET including the parasitic bipolar transistor for $V_{D'S'} > 0$.

Simulated breakdown characteristics of an n-MOSFET are shown in Fig. 2. The parameters used in the simulation are, $K_1 = 3.9$, $K_2 = 10\,\mathrm{V}$ $J_{0c} = 1.25 \times 10^{-10}\,\mathrm{A/m}$ and $r_{sub} = 4.0 \times 10^{-3}\,\Omega\mathrm{m}$. The I-V curve from device simulation shows hysteresis, i.e. the voltage which appears at the drain electrode at the upside of the current is higher than that at the downside. The circuit simulation result with $\tau_F = \tau_R = 0$, which corresponds to the original model[2], does not show the hysteresis. This leads to the underestimation of the voltage during ESD events. On the other hand, the result with $\tau_F = \tau_R = 0.5$ns clearly shows the hysteresis, which means that the charge storage effect at the base-emitter junction is considered correctly.

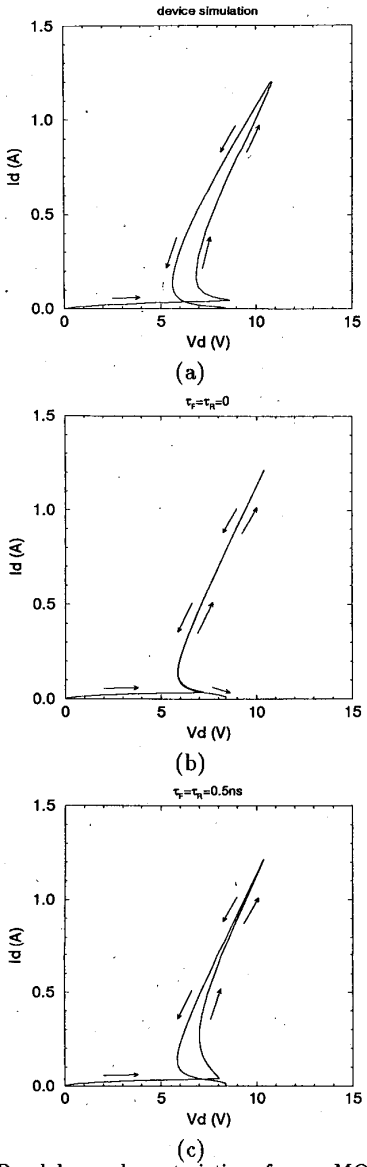

Fig. 2 Breakdown characteristics of an n-MOSFET under the ESD of the +2000V HBM: (a) device simulation, (b),(c) circuit simulation ($\tau_F = \tau_R = 0, 0.5$ns).

2.2 Lattice Heating

The current through devices causes Joule heating, which is dominant among several heating mechanisms[6]. Under ESD conditions, MOSFETs operate in saturation mode, and the potential difference between the source and the drain is mainly applied to the velocity saturation region of the length l_c. We assume that the heat generation occurs in the rectangular box, $\Delta = abc$, as shown in Fig. 3. This assumption is validated from the device simulation result shown in Fig. 4. Joule heating power in the box is expressed as $P(t) = V_{D'S'} I_D$. The temperature distribution is obtained using numerical integration of the closed form solution of a 3-dimensional thermal conduction equation in infinite medium[1]:

$$T(r,t) = T_0 + \zeta \int_0^t \frac{p(t)}{\rho c_p} G_1(x,a,t,\tau) \times G_1(y,b,t,\tau) \times G_1(z,c,t,\tau) d\tau, \quad (5)$$

$$G_1(\nu,\xi,t,\tau) = \frac{1}{2}\left\{ \mathrm{erf}\left(\frac{\xi/2+\nu}{2\sqrt{D(t-\tau)}}\right) + \mathrm{erf}\left(\frac{\xi/2-\nu}{2\sqrt{D(t-\tau)}}\right)\right\}, \quad (6)$$

where $p(t) = P(t)/\Delta$ and $D = \kappa/\rho c_p$. Note that D is assumed to be uniform throughout the device. The mass density $c_p = 2.32\,\mathrm{g/cm^3}$. The temperature dependence of the thermal conductivity $\kappa(\mathrm{W/cm\,K})$ and the specific heat capacity at constant pressure $c_p\,(\mathrm{J/cm^3K})$ are given as[7]

$$\kappa = 1/(0.03 + 1.56 \times 10^{-3} T + 1.65 \times 10^{-6} T^2), \quad (7)$$

$$c_p = 0.8509 + 1.522 \times 10^{-4} T - 1.582 \times 10^{4}/T^2, \quad (8)$$

where the temperature T is measured in K. These parameters are evaluated at the maximum temperature in the device. The effect of the smaller thermal conductivity of SiO_2, which is used in passivation layers, is considered by setting the empirical parameter, $\zeta = 1.1$. The solution shows isotropic temperature distribution around the heat generation region, which agrees with the result of device simulation shown in Fig. 5.

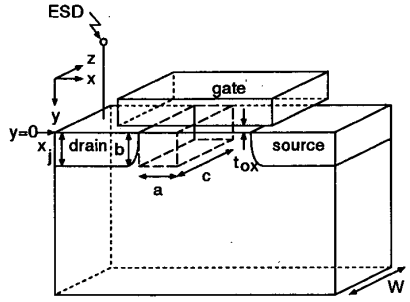

Fig. 3 The assumed heat generation region: $a = l_c$, $b = x_j$, $c = W$.

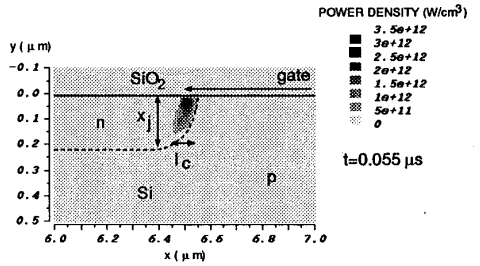

Fig. 4 The distribution of Joule heating, $J \cdot E$, from device simulation.

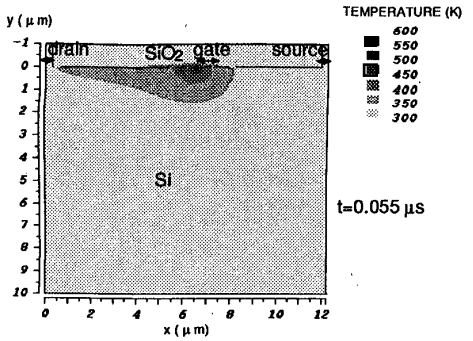

Fig. 5 The temperature distribution from device simulation.

Simulated total power and maximum temperature in the device are shown in Figs. 6 and 7, respectively. These figures suggest that the circuit simulation with thermal models described above correctly predicts the maximum temperature in the device under ESD conditions.

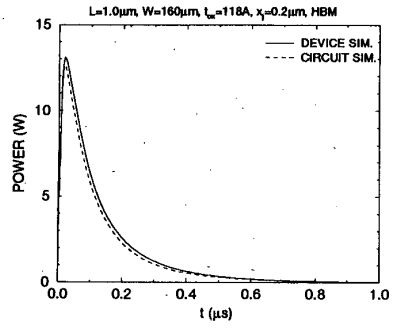

Fig. 6 The total power, $V_{DS}I_D$, dissipated in the device.

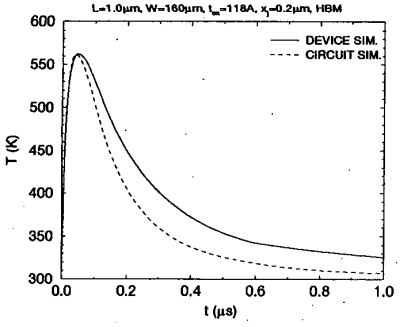

Fig. 7 The maximum temperature in the device.

3 Results and Discussion

The proposed electrothermal circuit simulator is applied to the ESD of the human body model (HBM) on an I/O circuit fabricated by a 0.25μm process. The circuit is schematically shown in Fig. 8. When the positive ESD voltage is applied, the current flows mainly through DQH transistors, as shown in Fig. 9. This is because the substrate voltage of these transistors is not directly tied to the ground and easily rises to induce bipolar transistor action. The current-voltage characteristic and the maximum temperature in the DQH transistors are shown in Figs. 10 and 11, respectively. The I-V curve shows a snapback characteristic, which indicates parasitic bipolar transistor action. The temperature is below 330K, so this circuit is prevented from thermal failure.

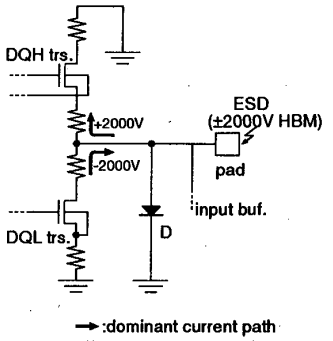

Fig. 8 Schematic diagram of the I/O circuit for ESD simulation. This circuit contains 75 MOSFETs.

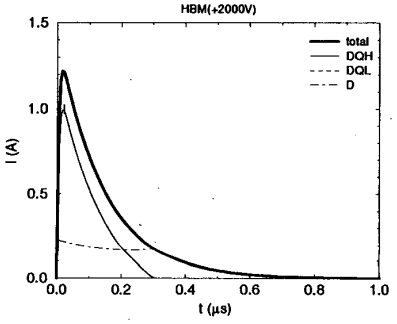

Fig. 9 The current waveform for the +2000V HBM.

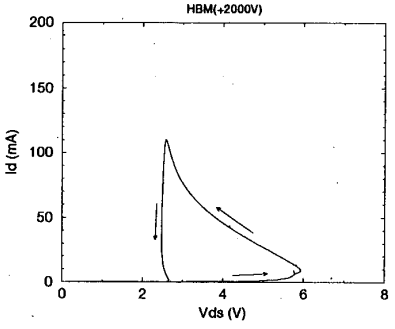

Fig. 10 The current-voltage characteristic in the DQH transistor for the +2000V HBM.

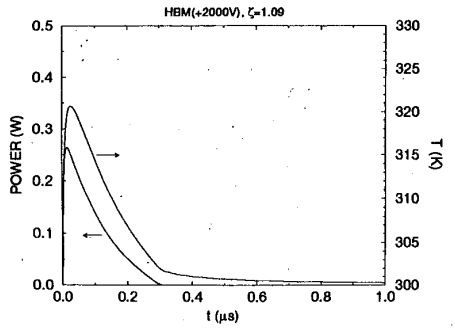

Fig. 11 The power, $V_{D'S'}I_D$, and the maximum temperature in the DQH transistor for the +2000V HBM.

In the case of negative voltage, the current flows mainly through DQL transistors, as shown in Fig. 12. This is because the substrate of the DQL transistors is directly tied to the ground and the current from the ground goes straight to the drain electrode through the forward-biased drain-substrate junction. The drain-source voltage during the ESD event is much lower than that in the case of positive voltage, so the temperature rise is smaller than that in the positive case, as shown in Figs. 13 and 14.

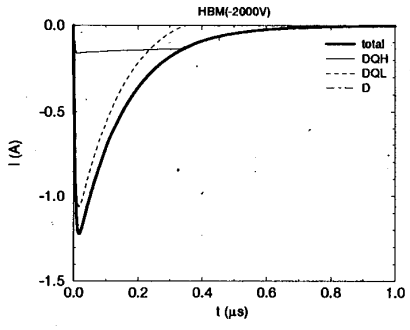

Fig. 12 The current waveform for the −2000V HBM.

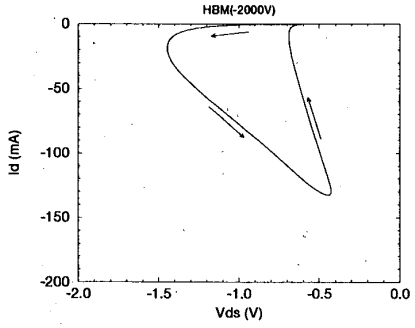

Fig. 13 The current-voltage characteristic in the DQL transistor for the −2000V HBM.

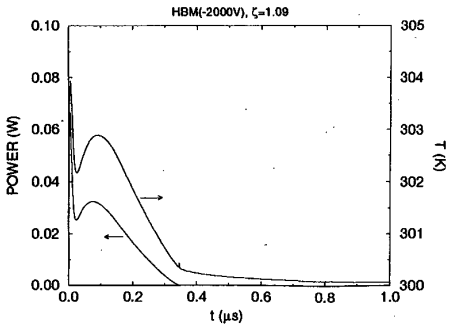

Fig. 14 The power, $V_{D'S'}I_D$, and the maximum temperature in the DQL transistor for the −2000V HBM.

From the above simulation results, we conclude that this circuit is proof against the ESD stress of the ±2000V HBM. In the ESD experiment, no functional failure was observed, which agrees with the prediction of the simulation.

4 Conclusion

We have presented an electrothermal simulation method suitable for circuit-level ESD analysis. Diffusion capacitance is introduced to cover the turn-on behavior of parasitic bipolar transistors. The temperature is also estimated from the resulting I-V characteristics. The calculated electrical and thermal characteristics agree well with the results of device simulation. The proposed method is useful in evaluating the ESD immunity of I/O circuits.

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