10-2

Precise Physical Modeling of the Reverse-Short-Channel Effect for Circuit Simulation

M. Suetake, M. Miura-Mattausch, H. J. Mattausch*, S. Kumashiro**, N. Shigyo**, S. Odanaka**, N. Nakayama**

Department of Electrical Engineering, *Research Center for Nanodevices and Systems, Hiroshima University

1-4-1, Kagamiyama, Higashi-Hiroshima, 739-8527, Japan

**Semiconductor Technology Academic Research Center

Onarimon BN Bldg., 16-10, Shimbashi 6-chome, Minato-ku, Tokyo 105-0004, Japan

Abstract

A Physical based threshold voltage model for circuit simulation is developed. The conventional short-channel effect as well as the reverse-short-channel effect are included. The reverse-short-channel effect due to impurity pileup at the surface of the substrate is modeled by assuming a linear impurity profile as a function of depth. Measured threshold voltage dependence on the bulk voltage is used to determine the impurity profile. The physically based modeling of the reverse-short-channel effect enabled a short-channel effect description, which simply exploits the channel length dependence of the lateral-electric field.

Introduction

The reverse-short-channel (RSC) effect is observed commonly in advanced n-MOSFET technologies, e.g. [1-3]. Its origin is a pileup of implanted B impurities at the SiO_2/Si interface under the gate [4]. A phenomenological model of the RSC effect on the threshold voltage V_{th} for circuit simulation has been proposed [5]. However, this model treats the effect by assuming fixed gate-oxide charges and neglects the real physical origin. We propose a new RSC effect model for circuit-simulation, which is based on a simplification of the B-pileup. The main task for a precise circuit simulation model of the RSC effect is a physically correct simplification of the 2D B-pileup phenomenon. In particular, the simplification of the impurity concentration must still lead to a physically meaningful carrier mobility in the channel region. Additionally 2D effects have to be efficiently transformed for inclusion into a circuit simulation model.

Modeling of V_{th}

Figure 1 shows 2D device simulation results of the threshold voltage (V_{th}) as a function of the gate length (L_{gate}) at the drain voltage V_{ds}=0.1V [6], for various substrate voltages V_{bs}. These results have been proved to reproduce measured characteristics satisfactory. Both the RSC effect and the short-channel (SC) effect are obvious. For modeling, V_{th} has to be partitioned according to these two effects as schematically shown in Fig.2, and thus V_{th} is written as

$$V_{th} = V_{thR} - delvth \tag{1}$$

where V_{thR} describes V_{th} including the RSC effect, and *delvth* is the V_{th} shift due to the pure SC effect.

Figure 3 shows the same results as Fig.1 but as a function of the square root of V_{bs}. An interesting feature of the plot is that the V_{th} values at $\sqrt{\phi_s - V_{bs}}$ =0 vary with L_{gate} and do not converge to the theoretically expected value of ϕ_s-V_{fb}. Here ϕ_s and V_{fb} are the surface potential at threshold condition and the flat-band voltage, respectively. To investigate the reason for this variation at $\sqrt{\phi_s - V_{bs}}$ =0 we have performed simulation experiments.

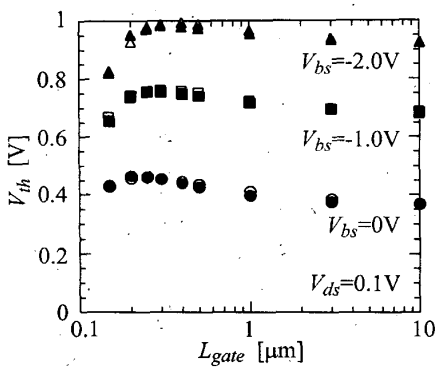

Fig. 1. Threshold voltage V_{th} as a function of the gate length L_{gate} for various substrate voltages V_{bs} at drain voltage V_{ds}=0.1V. Open symbols are 2D numerical simulation results and solid symbols are those calculated with the proposed model.

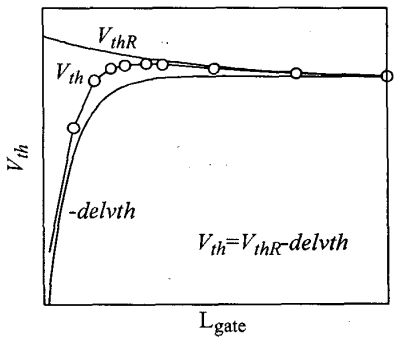

Fig. 2. Schematic of the V_{th} separation into the part originated by the reverse-short-channel effect V_{thR} and that by the short-channel efect delvth.

Figure 4 shows the four different vertical impurity profiles studied and Fig.5 shows the resulting V_{th} characteristics. The V_{th} values of all four profiles meet ,as expected, roughly at $\sqrt{\phi_s - V_{bs}}$ =0, and show a linear dependence on $\sqrt{\phi_s - V_{bs}}$ at normal operating conditions $V_{bs} \leqq 0$ of n-MOSFETs. If the V_{th} vs. $\sqrt{\phi_s - V_{bs}}$ characteristics for the two non-homogeneous profiles are also linearly extrapolated, V_{th} values at $\sqrt{\phi_s - V_{bs}}$ =0 converge obviously no more to the theoretical value. From these findings it is concluded, that the reason for the drastic change of V_{th} at $\sqrt{\phi_s - V_{bs}}$ =0 shown in Fig.3 can be explained by the linear extrapolation of the data and results from a N_{sub} distribution vertical to the surface. It has to be noticed additionally that the retro-graded profile results in an increased bulk coefficient and that the B-pileup suppresses this increase.

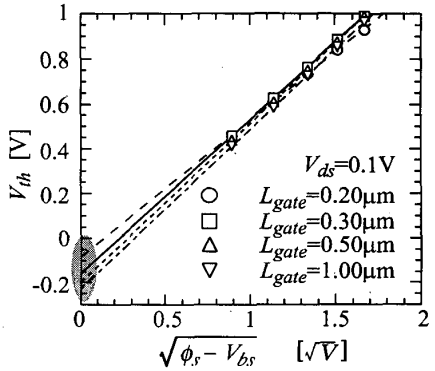

Fig. 3. The V_{th} values of Fig. 1 plotted as a function of $\sqrt{\phi_s - V_{bs}}$ for four different L_{gate} length.

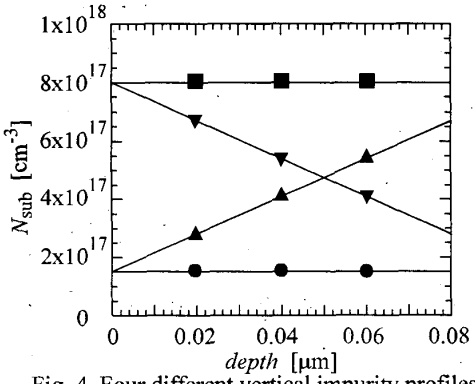

Fig. 4. Four different vertical impurity profiles shown by lines with different symbols as a function of depth. The profile with triangles corresponds to the retro-graded case, and that with inverse triangles to the B-pileup case.

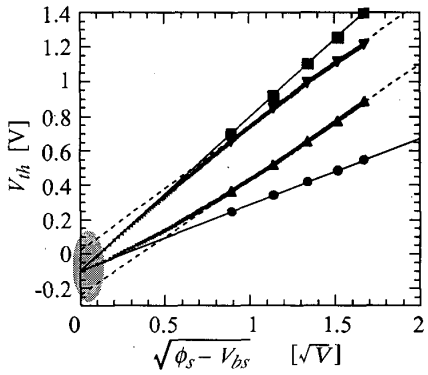

Fig. 5. Simulated V_{th} vs. $\sqrt{\phi_s - V_{bs}}$ characteristics of the four profiles given in Fig.4 with a 2D device simulater. Identical symbols as in Fig.4 are used for the corresponding profiles.

1) Characterization and Modeling of the RSC-Effect

Generally V_{th} is determined under the condition of a negligible inversion charge

$$V_{thR} = \phi_s + V_{fb} + \frac{Q_{dep}}{C_{ox}} \tag{2}$$

$$Q_{dep} = q \int_0^W N_{\mathrm{sub}}(x)\, dx \tag{3}$$

where W is the depletion width at threshold condition. For simplicity the 1D Poisson equation is solved under an approximation of a linear impurity profile N_{sub} as function of depth x to calculate the depletion charge Q_{dep}. The linear $N_{\mathrm{sub}}(x)$ profile is fitted so that simulated V_{th} vs. $\sqrt{\phi_s - V_{bs}}$ characteristics reproduce measured (or 2D simulated in our case) values. Thus a gate length dependent impurity model-profile $N_{\mathrm{sub}}(x, L_{gate})$ is obtained. However, circuit simulation model can not include the N_{sub} distribution vertical to the channel. Therefore in contrast to conventional modeling, $Q_{dep}(L_{gate})$ as determined from Eq. (3) is used for the circuit simulation model.

Usually a linear dependence of V_{th} on $\sqrt{\phi_s - V_{bs}}$ is observed, which leads to a linear dependence of Q_{dep} automatically from Eq. (2). This assumption is not severe as can be seen in Fig.5, since n-MOSFETs in circuits operate normally at $V_{bs} \leqq 0$.

2) Modeling of the SC effect

For short-channel transistors the SC effect has to be considered in addition to the RSC effect. The term responsible for the effect, *delvth* in Eq.(1), is written as

$$delvth = delvth0\,(S_1 + S_2\, V_{ds}) \tag{4}$$

$$delvth0 = \frac{2\varepsilon_{si}(V_{bi} - \phi_s)}{C_{ox}\,\alpha\,(L_{gate} - \beta)^2}\sqrt{\frac{2\varepsilon_{si}(\phi_s - V_{bs})}{qN_{\mathrm{sub}}(x=0)}} \tag{5}$$

where V_{bi} is the built-in potential between source/drain-contact and substrate, and C_{ox} is the gate-oxide capacitance per unit area. Here S_1, S_2, α, and β are parameters and have same meanings as in [7]. Equation (5) is derived by including the electric field E_y into Gauss' theorem

$$E_x + W\frac{dE_y}{dy} = -\frac{Q_{dep}}{\varepsilon_{si}} \tag{6}$$

$$delvth = \frac{\varepsilon_{si}}{C_{ox}}\, W\frac{dE_y}{dy} \tag{7}$$

where E_x is vertical electric field. In Eq.(5) the impurity concentration at the surface used to simplify the description. This simplification is not serious, since the gate length dependence dominates the effect.

Results

The obtained $N_{\mathrm{sub}}(x, L_{gate})$ profiles from the 2D simulated V_{th} vs. $\sqrt{\phi_s - V_{bs}}$ characteristics shown in Fig.1 and 3 are compared with input profiles used for the simulation in Fig.6. The vertical impurity profiles in the middle of the channel are depicted for the comparison. The discrepancy between the model N_{sub} and the exact 2D profile especially for long-channel cases is attributed to the selection of the position where the vertical 2D profiles are compared. Though we fixed the position in the middle of the channel, reality is varied according to the profile. Impurity profiles along the channel are not homogeneous but position dependent, and the whole distributions affect on the positions where V_{th} is determined. Calculated V_{th} values with these model profiles are depicted in Fig.1 by solid symbols. Separately calculated V_{thR} and

delvth are shown in Fig.7. For the V_{thR} values only $N_{sub}(x, L_{gate})$ is responsible. As can be seen from Eqs.4 and 5 totally only four model parameters are required for the *delvth* calculation. This surprisingly good result is due to the inclusion of the gate length dependent N_{sub}. Since the accuracy of the estimated $N_{sub}(x, L_{gate})$ has been proved as shown in Fig.6, the result given in Fig.7 should be accurate. The fact, that the SC effect can be modeled on the basis of a simplified description of its physical origin, suggests the possibility of this analytical model to be predictable.

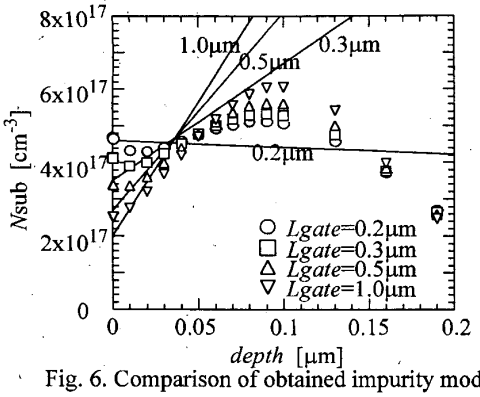

Fig. 6. Comparison of obtained impurity model-profiles from simulated V_{th} and those of 2D process simulation results used for the V_{th} simulation. Open symbols are 2D process simulation results in the middle of the channel, and lines are model profiles.

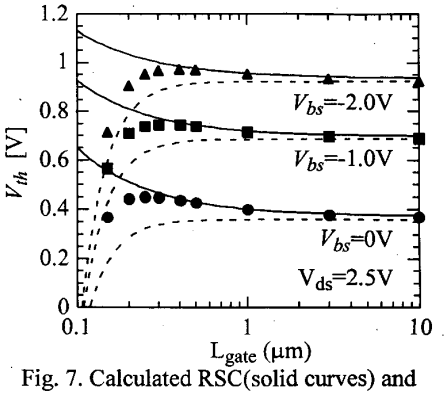

Fig. 7. Calculated RSC(solid curves) and SC(dashed curves) contributions to V_{th} as a function of L_{gate}. The calculated total V_{th} values are depicted together by solid symbols.

Conclusion

We have proposed a threshold voltage model describing the reverse-short-channel effect by approximating N_{sub} to be a linear function of depth. This model enables to reproduce complete V_{th} characteristics only with a few model parameters.

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