10-1 (Invited)

Interconnect Modeling for VLSI's

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1. Introduction

As scaling has been continued more than 20 years, it has yielded faster and denser chips with ever increasing functionality. The scaling will continue down to or beyond 0.1 μm as proposed in SIA Technical Roadmap [1]. With scaling, device performance improves, however, interconnect performance is degraded. Traditionally, IC circuit designers only consider device models in circuit simulations. In this scaled deep submicron technology, however, interconnects limit the performance, packing density and yield, if not properly modeled. With scaling, interconnect delay drastically increases and limits the length of global routing. The aspect ratio of interconnect increases and the coupling capacitance is dominating. Thus, the rapid increase of crosstalk will limit the scaling of interconnect pitches. In order to properly model and design the interconnect-dominated circuits, accurate and proper interconnect modeling is a must to assure the performance and functionality of ever-increasing complex multi-million transistor VLSI circuits.

Up to now, on-chip interconnect modeling only focuses the generation of 2-D/3-D interconnect model libraries using 2-D/3-D field solvers based on the interconnect geometry and material characteristics from the foundry's electrical design rules. Actually, interconnect modeling should oversee the overall flow of interconnect modeling in chip design to assure the accuracy of circuit simulations and eventually, the performance and functionality of IC chips.

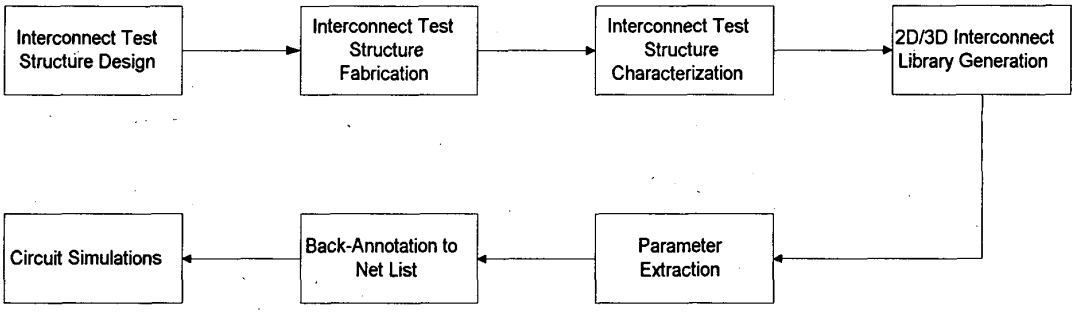

Figure 1. Overall Flow of Interconnect Modeling

Figure 1 illustrates the overall flow of interconnect modeling. It starts with the interconnect test structure (ITS) design. ITS is fabricated on silicon, measured, and characterized to extract the parameters of interconnect geometry and material characteristics (interconnect technology parameters). Due to the process variation, the spreads of the parameters are significant and affect the performance of IC circuits. Based on the characterized interconnect technology parameters(ITP), 2-D or 3-D interconnect model libraries are generated. Using these interconnect model libraries and device models, parameter extraction is performed on layout. Then, they are back-annotated to the netlist and circuit simulation are performed. The accuracy of the circuit simulation depends on the overall accuracy of this flow. Section 2 will explain the interconnect test structure(ITS) design, measurement, and characterization. In section 3, nominal interconnect modeling is illustrated using the 2-D/3-D field solvers, 2-D/3-D interconnect model libraries and parameter extractors. Until now, not much work has been done on the statistical modeling of interconnect. Section 4 will examine and explain the new development of statistical interconnect modeling. Section 5 will summarize and propose the future work in interconnect modeling.

2. Interconnect Characterization

Not much work has been done on on-chip interconnect characterization due to the short history of on-chip interconnect modeling. Standard characterization methods of metal lines and dielectric layers are used up to now. In order to measure and characterize the interconnect geometry and material characteristics, the interconnect test structures(ITS) should be designed and fabricated. The parameters characterized up to now are metal line width(W), metal line spacing(S), metal line thickness(T), metal resistivity(ρ), Inter-Layer Dielectic(ILD) thickness(H), and dielectric constant(ε). Detailed interconnect test structures and characterization methods are explained in reference [2]. More test structures and circuits are needed to calibrate the interconnect model library and parameter extractors. ITS should include practical line structures such as global lines or clock nets. Interconnect-dominated test circuits are also needed to calibrate the whole interconnect modeling procedure from characterization to circuit simulations. Usually, interconnect-dominated ring oscillators or inverter chains are used. However, more actual circuit blocks should be used to make the calibration more meaningful.

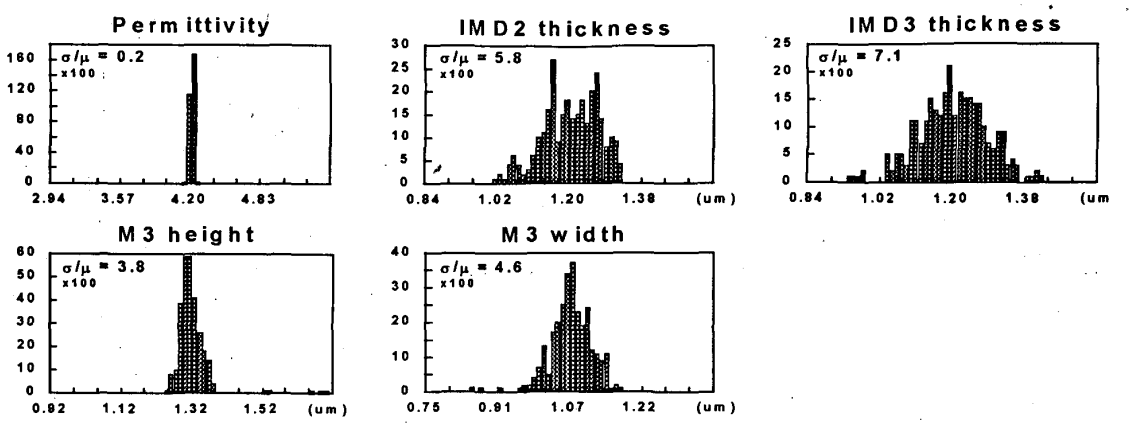

Figure 2. Measured distribution of Interconnect Technology Parameters

Due to the process variation, interconnect technology parameters(ITP) are varying substantially. Figure 2 shows the typical distribution of interconnect technology parameters. The variation is especially large in the ILD thickness and metal line width. Their variations have a definite impact to the total line capacitance and interline coupling capacitance and result in variation of the signal delay and crosstalk noise. The effect of the process variation should be modeled, because its impact on the signal delay and crosstalk is substantial. The conventional skew-corner worstcase modeling is too conservative. A new statistical interconnect modeling methodology will be discussed in Section 4. In the advanced interconnect technology, things are more complicated. Due to the smaller pitches, the offset of metal line width(delta-W) are not constant. It depends on metal pitches[3]. The ILD thickness depends on the underlying metal patterns. In the low K dielectric, the dielectric constant between the interconnect lines in the same layer is different from the dielectric constant between the interconnect layer. They are inhomogeneous and an-isotropic. Much more work should be done to characterize the interconnect geometry and material characteristics to assure the accuracy of interconnect modeling in the advanced interconnect technology.

3. Nominal Interconnect Modeling

Below several hundred MHz clock frequency, the inductive voltage drop is negligible compared with the resistive voltage drop in on-chip interconnect lines. Usually, on-chip interconnect lines are modeled as RC lines up to now without too much loss of accuracy. Still actual on-chip interconnect lines are too large and complicated to simulate by numerical field solvers. In order to overcome the problem, the interconnect model library-based parameter extraction methodology has been developed and used in IC industry. First, basic elements of interconnect lines are simulated and saved in the interconnect model library. Actual interconnect lines are decomposed into these basic elements and the R, C values of these elements are looked up at the interconnect model library. Using these R, C values, a netlist is assembled for back-annotation and circuit simulations. Above 1 μm generation technology, an interconnect line is considered as a capacitance load only. The interconnect line resistance is negligible compared with the device resistance. Aspect ratio is small and one-dimensional area capacitance approximation is enough. The total interconnect capacitance is extracted by the Boolean-operation based LPE tools using 1-D parallel-plate capacitance equation. Between 1 μm and 0.5 μm generation technologies, an edge fringing capacitance becomes significant, but a lateral coupling capacitance is not. All capacitance can be lumped to ground because the lateral capacitive coupling between lines is not significant. To calculate the total capacitance, it is enough to use 1-D area capacitances and 2-D fringing capacitances. Still the 3-D fringing is negligible. Interconnect parameter extraction is performed by quasi-3-D parameter extractors using 1-D and 2-D interconnect model libraries. 2-D model library is generated by 2-D field

solvers based on Finite-Difference Method(FDM), Finite-Element Method(FEM), or Boundary-Element Method(BEM).

Between 0.5 μm and 0.25 μm generations, aspect ratio becomes larger than 1. The lateral coupling capacitance is often larger than 50% of the total capacitance. Due to the large number of metal layers(> 3), 3-D fringing capacitance such as cross-over capacitance is significant. The resistance becomes an important component of delay. However, the inductance can usually be neglected. In order to model the capacitance properly, 3-D fringing should be considered. Many interconnect parameter extractors start to include the 3-D model library. There are a couple of issues in the 3-D model library. First, there are so many 3-D structures with multiple parameters. Only limited sets of 3-D structures can be includes due to the excessive man hours and CPU time to generate. In order to speed up 3-D library generation, fast 3-D field solvers have been developed such as Fast Multi-pole Method(FMM)[4] or Geometry Independent Measured Equation of Invariance(GIMEI)[5]. The other issue is errors introduced when 3-D nets are cut into 3-D structures. It can be avoided if the whole net and its neighbor are simulated at the same time. However, even fast 3-D field solvers based on discretization can not do the job because it generates multi-million-node matrix equations to solve. A new 3-D field solution method has been developed based on Monte Carlo simulation such as QuickCap[6] and Cap-Savior[7]. It can simulate the very long and complex global nets in VLSI chips within a reasonable time. The simulation time of Monte Carlo method is theoretically constant with respect to the geometry complexity. Thus, it is also attractive to the physical simulation problems such as inductance and thermal problems in the complex VLSI chips. In deep submicron designs, the number of transistors and interconnect increases drastically to or over multi-million. It becomes very time-consuming and memory intensive to extract interconnect parameters and to simulate them. It is a very challenging problem how to handle the exploding CPU time and memory requirement. It is also needed to simulate 3-D resistance structures using 3-D field solvers. However, it is not a problem because the number of 3-D resistance structures is relatively small. Below 0.18 um generation, the aspect ratio of interconnect lines approaches 2. The lateral coupling capacitance dominates the total capacitance; thus, delay and crosstalk noise. The inductance must be considered in cases such as clock nets, busses and power nets.[8]. The inductive coupling is long-range. It is also necessary to know the return path to model the inductance properly. It is a big challenge to model inductance in deep submicron VLSI chips.

4. Statistical Interconnect Modeling

As shown in Section 2, the interconnect technology parameters(ITP) such as ILD thickness and metal line width vary by more than 20%. Variations in interconnect capacitance and resistance are quite substantial and result in variations in the signal delay and crosstalk noise. The conventional interconnect worstcase modeling is based on the process skew corners. The probability of simultaneous occurrence of all 3-σ process skew corner values is much smaller than the 3-σ probability. Thus, the 3-σ values of R and C are quite conservative. Furthermore, R and C of interconnects are very strongly correlated. In order to take advantage of the independence of interconnect technology parameters(ITP), a root-sum-square method [9][10] has been proposed to estimate the R and C variation from the process skew corner values. It is successful to predict the 3-σ values of R and C, but it is not useful to predict the 3-σ values of the signal delay and crosstalk noise, because interconnect R and C values are strongly correlated.

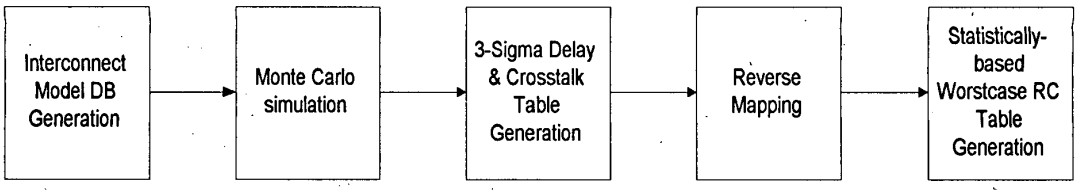

Figure 3. Flowchart of SWIM (Statistically-based Interconnect Worstcase Model generator)

A new statistically-based worstcase interconnect modeling method (SWIM) [11] has been proposed. It is based on Monte Carlo simulation. Its block diagram is illustrated in Figure 3. A multiple set of interconnect technology parameter values is randomly generated using 3-σ values of ITP assuming ITP has a normal distribution. Based on these randomly generated ITP values, the signal delay and crosstalk noise are calculated and their statistical distributions are determined. The 3-σ values of signal delay and crosstalk noise are determined from their statistical distributions. 3-σ delay or crosstalk worstcase R and C values are reverse-mapped to the corresponding ITP values. Thus, 3-σ worstcase values of signal delay and crosstalk noise can be predicted if these worstcase R and C values are used. Interconnect test structures including interconnect-dominated inverter chain is designed, fabricated, and characterized. 3-σ delay worstcase R and C values are generated based on SWIM. The interconnect-dominated inverter chains are simulated and compared with the measurement. Figure 4 shows the comparison of the simulations based on SWIM worstcase model and the measurement of signal delay. The 3-σ worstcase delay by SWIM is 20% larger than that of measurement. The overestimate by 20% is quite acceptable because some design margin is needed. The 3-σ delay of the skew-corner worstcase model is also calculated and plotted for comparison. It is 70% larger than

that of measurement. The statistically-based worstcase interconnect model improves 50% in estimating the 3-σ worstcase signal delay.

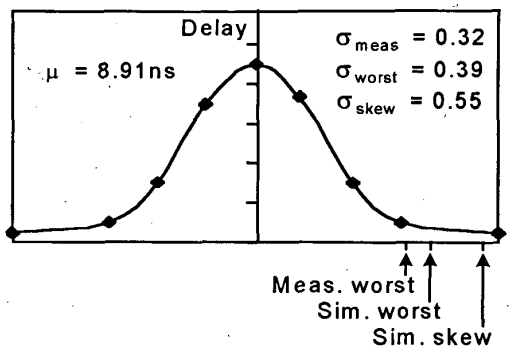

Figure 4. Comparison of inverter chain delays by measurement, skew-corner simulation, and SWIM-based simulation.

5. Summary

As scaling is continued down to deep submicron, interconnects become dominating the performance, signal integrity, and reliability of IC chips. However, due to the short history, not much work has been done on the overall interconnect modeling, especially interconnect characterization and statistical interconnect modeling. In interconnect characterization, more systematic methodology should be established in interconnect test structure design and their characterization. New test structures and characterization methods should be developed to characterize the advanced interconnect technology such as low K dielectric and copper. 2-D interconnect model library generation has been done by the 2-D Finite-Difference Method or Finite-Element Method. However, it takes too long to generate 3-D interconnect model library due to the increase of 3-D basic structures. Fast Multi-Pole Method(FMM)) [4] or Measured Equation of Inversion(MEI)[5] are used to speed up the 3-D library generation. To avoid errors due to 3-D structure partitioning, 3-D Monte Carlo Method is used to simulate the global nets. The ever-increasing clock frequency makes inductive effects more significant. However, it is very challenging to model the on-chip inductance due to its long-range interaction and wide return paths. Worstcase interconnect modeling has been done by the skew-corner method or root-sum-square method. Both methods are too conservative. Newly developed SWIM (Statistically-based Worstcase Interconnect Model generator) improves the worstcase delay within 20%. There have been significant progresses made in interconnect modeling, however, much more work should be done to model the coming advanced interconnect technology accurately.

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