An Accurate Compact Model for Ferroelectric Memory Field Effect Transistors

Marc Ullmann[1], Holger Goebel[1], Heinz Hoenigschmid[2], Thomas Haneder[3], Guido W. Dietz[4]

[1)] Institute of Electronics, University of the Federal Armed Forces, D-22043 Hamburg, Germany
[2)] Infineon Technologies AG, Semiconductor Group, Memory Products Division, D-81541 Munich, Germany
[3)]Infineon Technologies AG, Corporate Research, D-81730 Munich, Germany
[4)] Infineon Technologies Corp., Microelectronics, now Hopewell Junction, NY 12533, USA

Abstract
A new nonvolatile ferroelectric memory field effect transistor (FEMFET) compact model for circuit simulation is presented. Its analytical approach is based on the MOS capacitor equations taking into account the influence of a ferroelectric polarization. The accuracy of the description of the ferroelectric layer has been experimentally verified and the transistor model has been used to simulate a FEMFET cell array.

Introduction
Ferroelectric memories are an emerging technology since they combine small cell area and nonvolatile data storage as well as fast access-time. Besides the conventional 1T-1C cell the FEMFET memory cell, which requires only one transistor per memory cell, attracts more and more attention. The principle of a FEMFET is shown in figure 1a, b. The FEMFET is built up like a FET whose gate insulator consists of a ferroelectric layer. Additional dielectric layers may be added to prevent interactions between the substrate and the ferroelectric layer during fabrication.
As demonstrated in figure 1a, b the region of operation of the FEMFET at zero voltage depends on the value of the ferroelectric polarization P and thus on the polarity of a voltage pulse previously applied to the gate electrode. After applying a positive voltage pulse, the ferroelectric material is in the state of positive remanent polarization (Fig. 1a, marked with a dot). If the remanent polarization is large enough, the positive polarization charge at the bottom of the ferroelectric layer will be compensated by dopant ion charge and inversion charge, so that a conducting channel exists ("on state"). The "off state", where no conducting channel exists, appears after applying a negative voltage pulse to the gate. Due to the resulting negative remanent polarization charge the substrate is in accumulation. Consequently channel conductance can be controlled statically (nonvolatile) and can be used to define two logical states.
For the design of FEMFET memory devices it is essential to have an accurate circuit model which describes all important effects and which uses an efficient algorithm.
Models for ferroelectric devices presented so far either use implicit equations which must be solved numerically [1] or do not take into account correctly the history of the ferroelectric layer [1, 2, 3]. Furthermore, some models employ analytical descriptions which fail to accurately model hysteresis loops especially for low voltages [1, 2, 4].

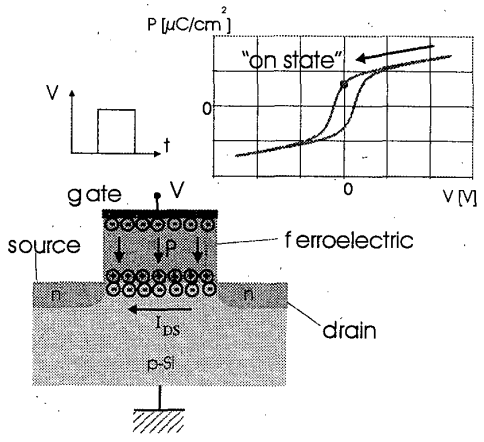

Fig. 1a: Structure of a FEMFET in inversion due to positive remanent polarization at zero bias. ("on state")

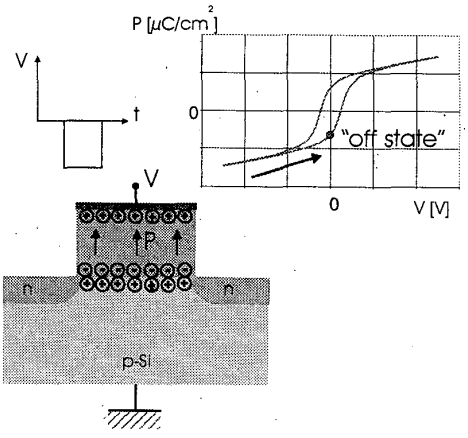

Fig. 1b: FEMFET in accumulation due to negative remanent polarization at zero bias. ("off state")

Modeling the ferroelectric field effect transistor

The current equation

The current I_{DS} between source and drain of a FEMFET can be determined, if the surface potential Φ_S at the dielectric-substrate interface at source and drain is known.

The presented model describes the relationship between the gate substrate voltage V_{GB} and the silicon surface potential Φ_s in terms of an effective gate-to-substrate voltage V_{GBeff}, that takes into consideration the history dependence of the gate ferroelectric.

$$\Phi_S = f(V_{GB}, P) = f(V_{GBeff}) \tag{1}$$

with P, the ferroelectric polarization and

$$V_{GBeff} = V_{GB} + \frac{t_f}{\varepsilon_0 \varepsilon_f} P. \tag{2}$$

Similar to the conventional FET, Φ_S is given by an implicit equation which can not be solved analytically. The equation for the surface potential Φ_{SX} at any position X of the channel solved for the effective gate to substrate voltage V_{GBeff} is given by [5]:

$$V_{GBeff} = V_{FB} + \Phi_{SX} + \gamma \sqrt{\Phi_{SX} + \frac{kT}{q} e^{\frac{q}{kT}(\Phi_{SX} - 2\Phi_F - V_{XB})}} \tag{3}$$

As pointed out time-consuming numeric methods have to be avoided in a circuit simulator. Hence the surface potential in the presented model is calculated by an approximation for MOS transistors described in [5]. For small effective gate to substrate voltages the electron charge is small compared to the depletion charge. Hence the exponential in (3) (resulting from the electron charge) is neglible and the surface potential in weak inversion is expressed by:

$$\Phi_{SX} \approx V_{GBeff} + \frac{\gamma^2}{2}\left[1 - \sqrt{1 + \frac{4}{\gamma^2}(V_{GBeff} - V_{FB})}\right]. \tag{4}$$

If the surface potential reaches values considerably bigger than $2\Phi_F + V_{XB}$, the exponential in (3) dominates and Φ_{SX} will be approximated in terms of V_{GBeff} by:

$$\Phi_{SX} \approx 2\Phi_F + V_{XB} + \frac{kT}{q} \ln(a + bV_{GBeff} + cV_{GBeff}^2). \tag{5}$$

To determine the coefficients a, b and c, three equations are required. The three equations are developed by fulfilling the following conditions.

Equation (5) and (4) must give the same value Φ_{SX} in the transition point $V_{GBeff} = V_{GBeff\,trans}$, with:

$$V_{GBeff\,trans} = V_{FB} + 2\Phi_F + V_{XB} + \gamma\sqrt{2\Phi_F + V_{XB}}. \tag{6}$$

Furthermore the derivatives of (5) and (4) have to be equal in the transition point. The third equation is obtained by choosing a second value of the surface potential, bigger than $2\Phi_F + V_{XB}$, that has to be equal to the exact value of equation (3). In [5], a value of $\Phi_{SX,2} = 2.5\Phi_F + V_{XB}$ is proposed.

The knowledge of Φ_{SX} is necessary to calculate the charges in the substrate and hence to determine the drain substrate current I_{DS}. The current flow in the transistor is caused by free charges (electrons for an n-channel device) in the inversion layer. If we make use of the familiar charge-sheet approximation, due to the very thin inversion layer thickness, we can calculate the carrier density per unit area in two ways [5]:

1. From the difference of the electric fields, caused by the total substrate charge and the dopant ion charge, the charge σ per unit area due to the electron density of the inversion layer becomes :

$$\sigma = -c_{ox}\left(\sqrt{\Phi_{SX} + \frac{kT}{q} e^{\frac{q}{kT}(\Phi_{SX} - 2\Phi_F - V_{XB})}} - \sqrt{\Phi_{SX}}\right). \tag{7}$$

2. The difference of the charge displacements, that results from the voltage loss across the gate insulator and the ions respectively, yields:

$$\sigma = -\gamma c_{ox}\left[(V_{GBeff} - V_{FB} - \Phi_{SX}) - \gamma\sqrt{\Phi_{SX}}\right]. \tag{8}$$

The transistor current I_{DS} is composed of a drift and a diffusion component as follows:

$$I_{DS} = W\mu\left(\underbrace{\sigma E_x}_{drift} + \underbrace{\frac{kT}{q}\frac{d\sigma}{dx}}_{diffusion}\right). \tag{9}$$

After integrating (9) from source (S) to Drain (D) with equation (8) and $d\Phi_{SX}/dx = -E_X$, one obtains the following expression for the drain source current:

$$I_{DS} = \frac{W}{L}\mu c_{ox}\left[\left(V_{GBeff} - V_{FB}\right)\left(\Phi_{SD} - \Phi_{SS}\right) - \frac{1}{2}\left(\Phi_{SD}^2 - \Phi_{SS}^2\right) - \frac{2}{3}\gamma\left(\Phi_{SD}^{\frac{3}{2}} - \Phi_{SS}^{\frac{3}{2}}\right) + \frac{1}{c_{ox}}\frac{kT}{q}\left(\sigma_D - \sigma_S\right)\right]. \tag{10}$$

By substituting equation (2), (4, 5) and (7) in (10), the resulting equation describes the drain source current for all regions of transition. Using this approach for the FEMFET model yields an accurate approximation of the drain source current I_{DS}. Figure 2 shows a comparison of the results calculated by the used approximation and the time consuming numerical solution.

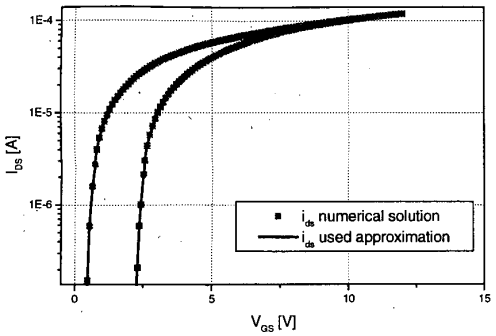

Fig. 2 : Comparison of I_{DS}-V_{GS} for the numerical solution and the approximation used in the model.

Calculating the Hysteresis

The insulator structure of the presented FEMFET model consists of one ferroelectric layer and one dielectric buffer layer that prevents interactions between the substrate and the ferroelectric material during processing. The ferroelectric layer can be described as a parallel element built by a linear capacitor and a pure ferroelectric one [1]. This leads to the following equation, that is generally valid for dielectric materials:

$$D = \varepsilon_0\varepsilon_r E + P\,. \tag{11}$$

The necessity for an accurate handling of the ferroelectric history is taken into consideration by using a computationally efficient implementation including history subcycle scaling as described in [4] for ferroelectric capacitors.

The ferroelectric hysteresis curves have to fulfill three conditions. First of all, any *P-V* point must always lie on or within the saturated hysteresis loop. Secondly, the derivative dP/dV is always less or equal dP_{sat}/dV of the belonging saturated branch. Thirdly, leaving a sub loop to higher (ascending branches) or lower voltages (descending branches) than the starting turning point of the sub loop, the *P-V* curve passes always through this starting turning point. These three conditions can be fulfilled by describing the saturated loop with an empirical mathematical fitting function. The ascending (descending) sub loop branches are always a fraction of the saturation loop at the same voltage *V* [4]. This approach for calculating the ferroelectric polarization *P* is based on the Preisach model and has been adapted to the FEMFET model. Yet the hyperbolic tangent function used in [4] is replaced by an arcus tangent function that fits the experimental loops more accurately, especially for low voltages [6].

Results

The presented FEMFET model has been implemented into the Saber circuit simulator. The simulation results of the ferroelectric hysteresis loops were compared with measurements on $SrBi_2Ta_2O_9$ thin film capacitors with Pt electrodes. The thickness of the SBT film was t_{fe} = 180 nm. The results show an accurate correspondence even at low voltages (Figure 3).

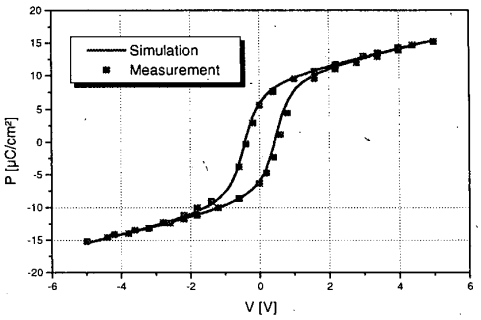

Fig. 3: Comparison of simulation and experimental data (polarization of a 180 nm thick SBT capacitor)

Another example, which shows the usefulness of the model, is the simulation of a FEMFET memory cell array (Figure 4). The used device parameters are shown in Table 1. Figure 5 presents the simulation result of a write operation on the selected cell T_0_1 (saturated loop) and the problematic sub loops occurring at cells T_0_0 and T_1_1.

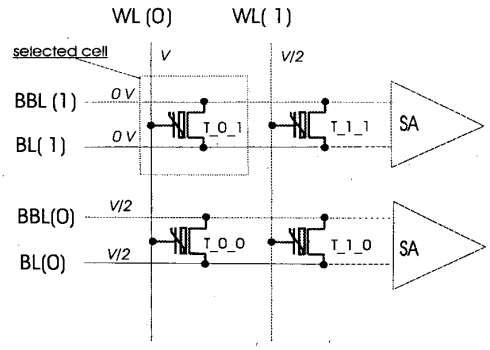

Fig. 4: FEMFET cell array during a write operation on T_0_1.

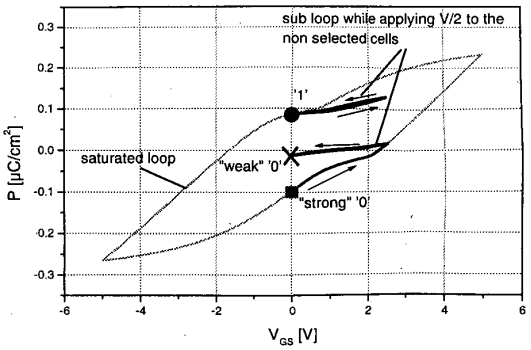

Fig. 5: Simulation of write operation on a FEMFET cell array.

If the common *V*/2–rule for a write operation [7] is used, the write voltage *V* is applied to memory cell T_0_1, amounting to a stored '1'. Furthermore a voltage of *V*/2 is applied to memory cells T_0_0 and T_1_1 even if these cells are not selected. (In figure 4 the applied voltages are printed in italics). This does not affect a stored '1', but it weakens a stored '0' in the non selected cells due to resulting sub loops as shown in figure 5.

Parameter	Value	Unit
P_s	0.1	µC/cm²
P_r	0.08	µC/cm²
Ec	20	kV/cm
t_{fe}	180	nm
t_{ox}	20	nm
ε_f	92	
ε_{ox}	20	
A	$2*10^4$	µm²
N_A	$2*10^{15}$	cm^{-3}
V_{FB}	-1.0	V
V_D	0.1	V
V_S	0	V
V_B	0	V

Table 1: FEMFET device parameters.

Conclusion

A ferroelectric memory field effect transistor model based on semiconductor physics for use in circuit simulators has been developed and demonstrated on a simple memory cell array. The approximation of the surface potential Φ_S leads to an efficient analytical description of the drain source current I_{DS}. The simulation results may not only be used for testing different VLSI memory architectures, but also to support the understanding of device properties and their dependence on geometry and material.

List of symbols

c_{ox} = oxide capacitance per unit area (F/m²)
k = Boltzmann's constant (J/K).
t_{fe} = ferroelectric layer thickness (m).
t_{ox} = oxide layer thickness (m).
E_c = coercive field (V/m).
E_x = horizontal electric field (V/m).
I_{DS} = drain to source current (channel current) (A).
N_A = substrate doping concentration (m^{-3}).
P = ferroelectric polarization (C/m²).
P_r = remanent polarization (C/m²).
P_s = spontaneous polarization (C/m²).
q = magnitude of electronic charge (C).
T = absolute Temperature (K).
V_{GB} = applied gate to substrate voltage (V).
V_{XB} = voltage along the channel (V).
V_{FB} = flat band voltage (V).
γ= body effect coefficient ($\sqrt{V}$).
ε_0 = permittivity of free space (F/m).
ε_f = permittivity of the ferroelectric.
ε_{ox} = permittivity of the oxide (F/m).
Φ_{SX} = surface potential along the channel (V).
σ= inversion layer electron density per unit area (C/m²).

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