Modeling of direct tunneling gate current in ultra-thin gate oxide MOSFETs: a comparison between simulators

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Abstract

The direct tunneling (DT) current through the 1.5 nm gate oxide layer of a 0.07 μm channel length n-MOSFET is calculated using the semi-classical approximation of electron transport. The quantities needed for this calculation are extracted from three types of device simulation based on either Drift-Diffusion, Energy-Balance, or Monte Carlo transport model, for comparison. The maximum gate current is obtained for $V_{GS}=V_{DD}$ and $V_{DS}=0$, *i.e.*, a static point of CMOS inverter. It is shown that the DT effect is dominated by near-thermal electrons injected at the source side of the channel. As a consequence a good agreement is found between DT calculations from the three simulators, in spite of very different physical descriptions at the microscopic level.

1. Introduction

With the scaling down of the MOSFET into the sub-100 nm regime, the gate oxide thickness is expected to enter the sub-3 nm range in order to ensure an effective channel control. Indeed, excellent electrical performance has been obtained for 1.5 nm oxide MOSFETs [1]. Nevertheless, such ultra-thin gate oxide gives rise to a significant direct tunneling (DT) gate current, likely to cause severe problems of power consumption and oxide reliability. Study and modeling of DT gate current in MOSFETs is thus an important issue for designing future CMOS technology. Generally speaking, the calculation of DT current density along the channel requires the knowledge of some microscopic quantities, *e.g.* oxide field and carrier distribution function, which can be extracted only from 2D device simulation. It has been shown for thick gate oxide MOSFETs (>3 nm) that injection into SiO_2, which is dominated by assisted tunneling, thermoionic emission, or Fowler-Nordheim tunneling, is closely related to the carrier heating in the channel. Within this context, the aim of this paper is to reinvestigate in the DT regime the influence of the carrier energy distribution on gate leakage. For this reason, DT gate currents of a typical ultra-short gate MOSFET are calculated using data extracted from three types of device simulator based on different approaches of the Boltzmann transport equation solution. In order of increasing accuracy we use Drift-Diffusion (DD) [2], Energy-Balance (EB) [2], and Monte Carlo (MC) [3] transport models, the latter being used as a reference. The critical comparison of results must decide whether DD and/or EB device simulators can give correct estimates of gate current in ultra-thin gate oxide MOSFETs in spite of simplified carrier transport description, while saving CPU time. The simulated device is a 70nm N-channel length MOSFET with a 1.5 nm thick gate oxide. A uniform substrate doping of $10^{18}cm^{-3}$ is assumed.

2. Method of gate current calculation

DT currents are calculated within the semi-classical approximation of electron transport as the product of the charge flows at the Si/SiO_2 and $metal/SiO_2$ interfaces by the transmission probability. Rigorously, this calculation should be included in the simulators as a new condition at interfaces. But with maximum gate current of some A/cm^2 [1], the charge

injection through the oxide is expected to weakly perturb the transistor state, which allows using a post-simulation procedure for DT calculation from microscopic data provided by simulation.

The transmission probability is calculated along the channel using the transfer-matrix solution of the Schrödinger equation [4]. In agreement with experimental works, the parallel wave vector conservation is relaxed [5]. This assumption reduces the calculation to a 1D problem depending on the perpendicular kinetic energy ε_x and the barrier shape. The transmission probability is hereafter noted $P(y,\varepsilon_x)$, where y is the position along the channel. The conduction band offset at the Si/SiO_2 interface and the electron effective mass in SiO_2 are assumed to be 3.1eV and $0.5m_0$, respectively [5]. The image potential correction is neglected.

Using Monte Carlo simulation, the electron flow $d\Phi(y,\varepsilon_x)$ at Si/SiO_2 interface is obtained by recording each electron hitting the interface during the simulation time [6]. The current density at position y is then given by

$$J_G(y) = q\int_0^{+\infty} P(y,\varepsilon_x)\, d\Phi(y,\varepsilon_x) \qquad (1)$$

Using DD and EB simulation, the electron flows are deduced from the analytic distribution functions taken into account in this kind of simulator. The Boltzmann statistics is used in this work to be consistent with the present Monte Carlo model that does not treat electrons as fermions. Assuming parabolic energy bands, the flow of electrons hitting the Si/SiO_2 interface at position y with a normal kinetic energy ε_x can be expressed as

$$d\Phi(y,\varepsilon_x) = \frac{m^*_{DS} k_B T_C(y)}{2\pi^2\hbar^3} \exp\left(-\frac{(E_C - E_F)_i(y)}{k_B T_C(y)}\right) \exp\left(-\frac{\varepsilon_x}{k_B T_C(y)}\right) d\varepsilon_x \qquad (2)$$

In this expression, $(E_C - E_F)_i(y)$ is the local difference between the Fermi level and the bottom of conduction band at the interface, and $T_C(y)$ is either the lattice (DD) or the carrier (EB) local temperature. The bottom of conduction band in Si is formed by six ellipsoidal Δ valleys with a longitudinal mass $m^*_l = 0.92\ m_0$ and a transverse mass $m^*_t = 0.19\ m_0$. In case of a <100> silicon orientation, the total density of states mass to be used for carrier flow calculation is $m^*_{DS} = 2m^*_t + 4\sqrt{m^*_t\, m^*_l} = 2.05m_0$. The current density is then obtained by applying Eq.(1) with substituting for $d\Phi$ from Eq.(2).

Tunnel injection from metal (N doped poly-silicon) to silicon is similarly calculated, but assuming an electron distribution at thermal equilibrium (Fermi statistics) in the gate metal with a single energy band described by an effective mass $m^*_{DS}=m_0$. The post-calculation is strictly the same from MC, DD, or EB simulation.

3. Results and discussion

As preliminary result, we plot in Fig.1 the gate current as a function of gate voltage at $V_{DS}=0$, *i.e.*, without influence of transport model, obtained from both DD/EB (dashed line) and MC simulation (solid line). We observe a close agreement between both curves, which proves the consistency of the different approaches used to calculate DT gate currents and the correctness of the density of states mass used in Eq.(2). This is a satisfying basis for further comparisons at positive V_{DS}.

We plot in Fig.2 the gate current versus drain voltage characteristics at $V_{GS}=1V$ obtained from the three device simulators. Fig.2 exhibits two surprising results. The first one is the gate current decrease when raising V_{DS}. As a consequence, the maximum gate leakage

current is obtained for one of the two static points of CMOS inverters, *i.e.*, for $V_{GS}=V_{DD}$ and $V_{DS}=0$, which induces new constraints to MOSFET scaling related to static power consumption of CMOS circuits. The second surprising result is the relative agreement between gate currents obtained from the three kinds of device simulation. These results can be understood by comparing the DD, EB, and MC electron flows at the Si/SiO_2 interface and transmission probabilities plotted in Figs.3 and 4 for the bias point of maximum drive current, *i.e.*, at $V_{GS}=V_{DS}=V_{DD}=1V$.

Figs. 3 a) and 3 b) show the DD, EB, and MC electron flows versus electron perpendicular kinetic energy ε_x, at two channel positions, *i.e.* at the channel middle and near drain, respectively. The three device simulators give quite dissimilar flow shapes, as waited due to the different transport models associated. We observe that the carrier flow at low ε_x, is overestimated with DD simulation, which is related to the poor validity of the DD model at the microscopic level for such ultra-short MOSFETs. We also see that the carrier temperature approach of EB enables to roughly fit the MC electron flow at small perpendicular energy but leads to a severe overestimate of the high energy tail. Consider now the transmission probabilities plotted in Figs. 4 a) and 4 b) at the same channel positions. We observe that the probabilities calculated from DD, EB, and MC simulators do not strongly differ, which is mainly due to roughly identical oxide electric fields. But one of the most important point to note is that electrons moving from source to drain have to face a less and less transparent potential barrier. This tendency, which is due to the barrier deformation from a triangular shape near source to an almost rectangular shape near drain when $V_{DS}=V_{GS}$, acts as a strong limiting effect to hot carrier injection into SiO_2 in case of ultra-thin gate oxide MOSFETs. Actually, the barrier potential effect is stronger than the carrier heating phenomena, as shown by the collation of Figs.3 a) and 3 b). In other words, the injection of hot carriers near drain is not effective and the DT current is dominated by near-thermal electrons at the source side of the channel. At $V_{DS}=V_{GS}=1V$, current density is about $4A/cm^2$ near source and only $0.1A/cm^2$ near drain. This explains (i) the decrease of DT gate leakage observed when increasing V_{DS}, and (ii) the fact that gate currents obtained from DD, EB, and MC data are so weakly different.

4. Conclusion

A good agreement is found between DT gate currents obtained from DD, EB, and MC simulation of a 0.07 μm-channel length n-MOSFET with 1.5 nm-thick gate oxide. The electron energy distribution functions at the Si/SiO_2 interface strongly differ, as waited due to non-stationary effects and hot carrier phenomena, but it is shown that the carrier heating is far too small to counterbalance the potential barrier hardening at the channel end. Contrary to the case of thicker oxide, DT through SiO_2 is dominated by near-thermal carriers mainly injected near the source well. The exact shape of the carrier energy distribution at the Si/SiO_2 interface is thus not necessary to a rough estimate of DT gate current. Finally, it is found that the maximum gate leakage is obtained for one of the two static points of CMOS inverter, *i.e.*, for $V_{GS}=V_{DD}$ and $V_{DS}=0$.

References

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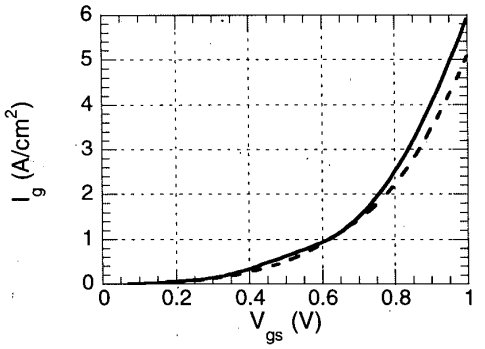

Figure 1: DD/EB (dashed line) and MC (solid line) gate currents versus gate voltage characteristic at V_{ds}=0.

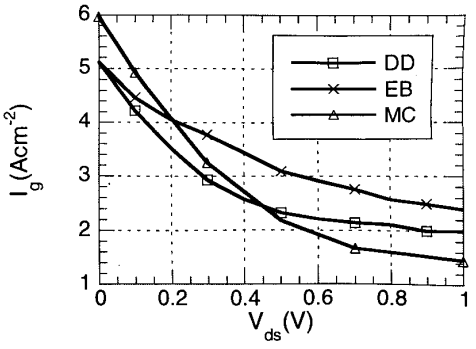

Figure 2: Gate current versus drain voltage characteristic from DD, EB, and MC simulation at V_{gs}=1 V.

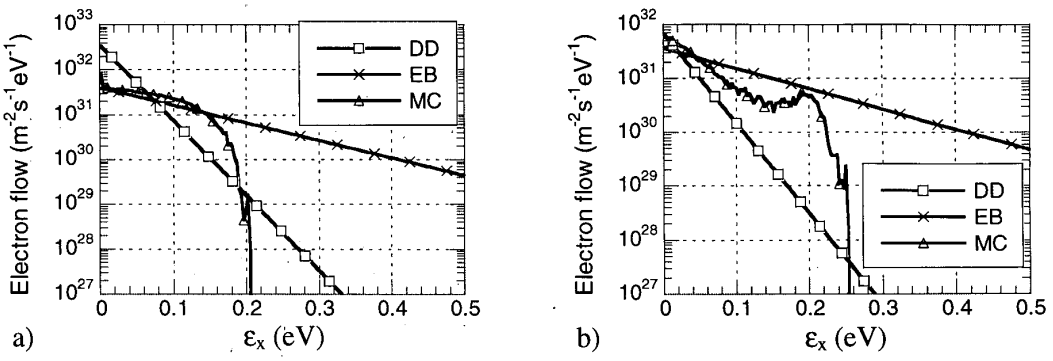

Figure 3: Electron flow versus electron kinetic perpendicular energy at V_{gs}=V_{ds}=1 V: a) at the channel middle, b) near drain.

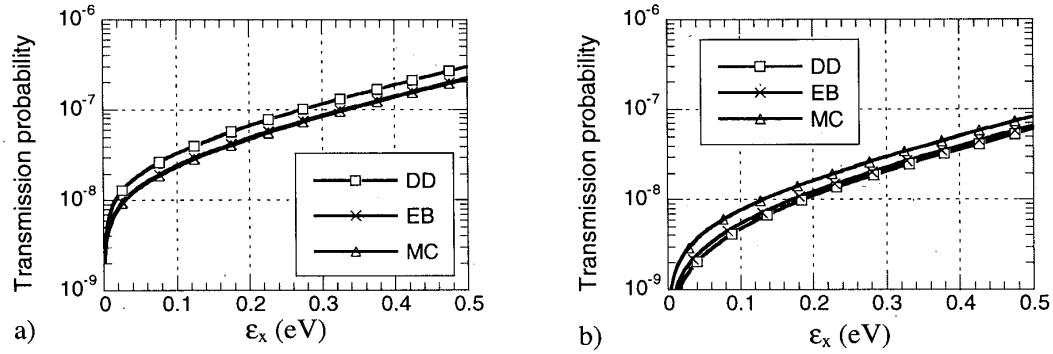

Figure 4: Transmission probability versus electron kinetic perpendicular energy at V_{gs}=V_{ds}=1 V: a) at the channel middle, b) near drain.