6-4

An Efficient and Accurate Delay Library Generation with RSM

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Abstract

In MPU/ASIC design with 0.2 μm BiCMOS LSIs, it is well known that interconnect delay becomes one of the key data to ensure high operating frequency. To verify the whole path delay accurately, one needs to create huge delay and waveform libraries which reflect updated process and interconnect structure as well as device performance. Because of the necessity for more than 100k times of CKT simulation to create the libraries, it was impossible to update the library quickly including process variation effects. In this paper, we have proposed a realistic new method to generate the libraries, 100 times faster without loosing accuracy. In application for a BiCMOS ASIC process, we have verified that the new method has achieved a reduced library creation-time of 1/100 within the delay error of 3%. This technique can be used in our TCAD/DA framework[1], which gives a predictive TCAD generation of delay-libraries in concurrent ASIC system and process development.

1. Introduction

It is known that there are major two problems in updated MPU/ASIC system and chip development. One is design productivity of millions gate in a SoC (System-on-a-Chip), in which reuse-methodology of pre-verified cores has been extensively studied to overcome the problem. The other is various analog characteristics in a high speed analog and digital circuits such as delays, noises in Vss/Vdd/Substrate and reliability problems. In sub-quarter μm CMOS process, interconnect delay becomes one of the key design issues to ensure high operating frequency, since increasing requirement for high-speed operation (clocking) forces a precise clock-distribution design as well as accurate gate and interconnect delay estimation.

In this work, we have proposed an accurate delay model and its efficient delay-library generation method with newly introduced RSM (Response Surface Method) technique. It allows a quick delay-library generation with reasonable accuracy.

2. System and Methodology

Fig. 1 shows the scheme of delay library generation. In the conventional method, the delay library has been constructed through the use of table-look up approach. In this method, each table has been computed using circuit simulation with pre-determined process/device and interconnect model parameters. Process/device parameters can be determined through TCAD simulations at desk-top process design phase and also can be extracted with electrical test data of chip fabrication. Interconnect delay model, in our work, contains four independent model-parameters to ensure pico-seconds accuracy of gate and interconnect delay estimation. Therefore, 400k-cases calculations of circuit simulation have to be done to generate typical delay-library, which requires about one month CPUs on 5 high-end EWS!

Fig. 2 shows the delay model used in this work, which calculates propagation delay time as well as output slew rate as functions of four parameters. The parameters are the input slew rate(tr/tf), capacitance (C1 & C2) and resistance (R) [2]. Table 1 summarizes these parameters and eight-types of delay & waveform table data, which are used in a 0.2μm BiCMOS process library.

Fig.3 demonstrates the simulation points for both conventional method and new RSM in case of three design-variables. In conventional method, as shown in the figure, circuit simulations have to be done on each 3D mesh point and the exact delay value on X, Y, Z-space is calculated by the linear interpolation using the constructed three-dimensional table. On the other hand, in the proposed method, each delay type is described as the quadratic Response Surface Function (RSF) with C1, C2, R and input slew rate. BBN (Box Behnken), CCF (Central Composite Faced) and combination of CCF and BBN design tables were studied to create the RSFs, in which all of these design table need a very small numbers of simulations as shown in the Figure. As a result, BBN was found to be optimized for all type of RSFs which achieve less than 3% average errors. Since these ranges of parameters are usually very wide, it is difficult to express with one RSF for whole range in some cases. In order to improve accuracy (reduction of the maximum error), we have investigated a lot of combination of RSFs and transformation of variables for all the delay types. The selected points for each design table are optimized to create the accurate RSFs. To decrease the simulation works, the separated range is determined to be the same area for all delay types.

3. Experiments

Fig. 4 shows maximum errors for RSFs of tr/tf (ff) which were obtained by using three design tables (BBN, CCF, BBN+CCF). The number of simulations was 25, 25 and 41 in BBN, CCF and the combination of BBN with CCF, respectively. BBN was chosen as a design table to create RSF since BBN has given the least maximum error for the tr/tf (ff) estimation. In our work, 18 RSFs were determined to express the whole delay types, which results in less than 20% maximum and 3% average errors without using variable transformation technique. Fig. 5 shows the average and maximum errors of eight delay types with the number of RSF=18. The errors were obtained on the basis of the 9000 data for each delay type which were calculated by circuit simulation. As shown in the figure, every delay type is within an average error of 3% using the 18 RSFs. The maximum error was obtained about 20%, in which only 0.1% of 9000 data shows >5% errors. Further study on optimized transformation technique has proven that only 4 RSFs were able to predict the tr/tf (ff) with an average error of 3% as shown in Fig. 6. In this case, input slew rate and C1 are transformed into the square functions. Fig. 7 shows relative CPU time dependence on number of RSF. The CPU time of the conventional table look-up method is assumed to be 100%. The proposed method has reduced the simulation works to about 1/100 within an average error of 3% , when compared with conventional delay-table construction method.

4. Conclusion

We have proposed an efficient and accurate delay library generation strategy with applied RSM. It has achieved a hundred times faster creation of the delay libraries of a 0.2μm BiCMOS process within an average error of less than 3%. This new technology can be utilized in our TCAD/DA methodology which allows a predictive chip-design with quick quantitative delay parameters and libraries required in DA works.

References
[1] H. Masuda et al.; Tech. Digest of ASP-DAC'98, pp.129-134, 1998.
[2] Y. Miki; IEICE Trans. Fundamentals., Vol. E79-A, p2117, 1996.

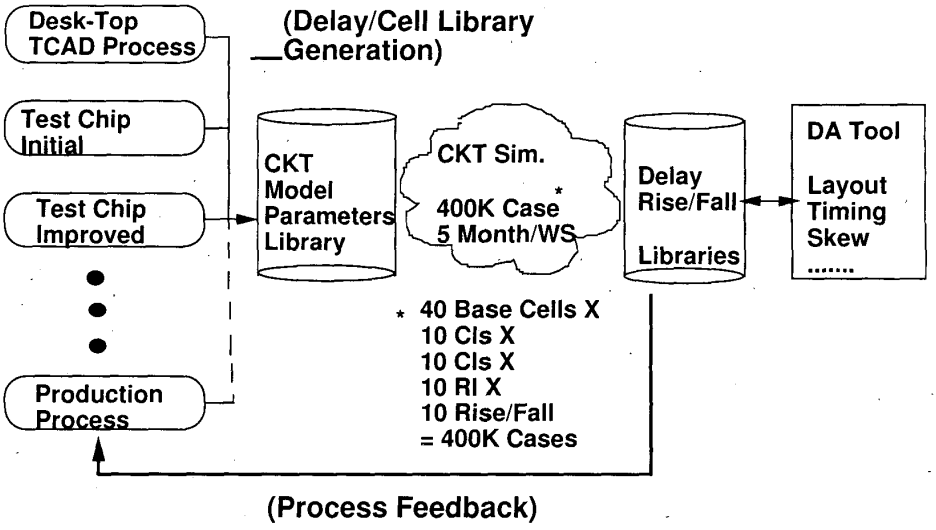


Fig. 1 Scheme of Delay Library Generation

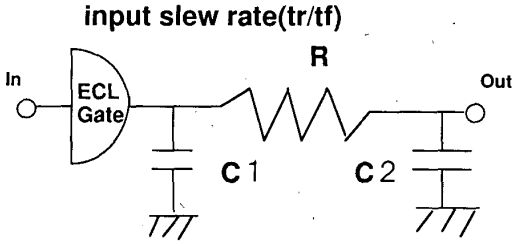
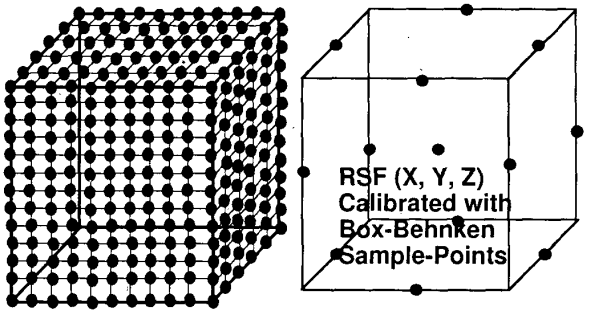


Fig. 2 Circuit delay model

Table 1 Parameters and Delay table

Parameters	input rise/fall time C1,C2 R
Delay table data	CKT types tpd (f f, f r, r f, r r) slew rate (tr/tf) (f f, f r, r f, r r)



(a) Conventional method (b) RSM

Fig. 3 Simulation points

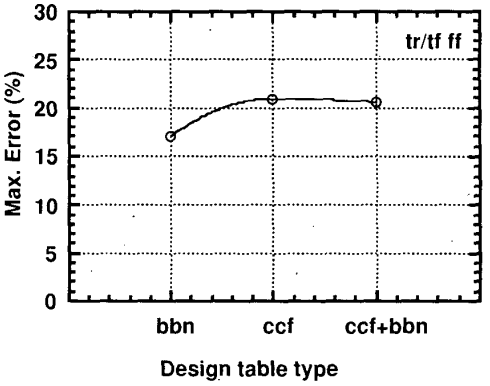


Fig.4 Maximum error for each design table type

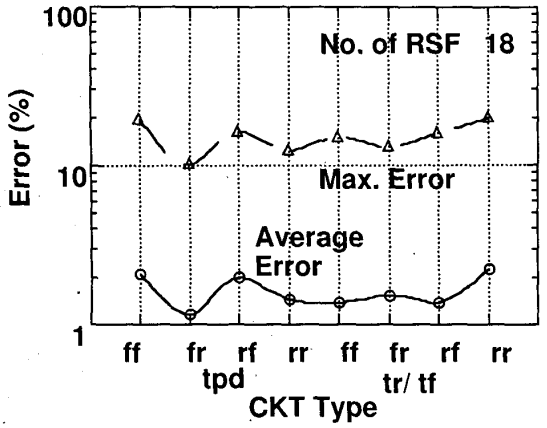


Fig. 5 Average and maximum errors for each delay type

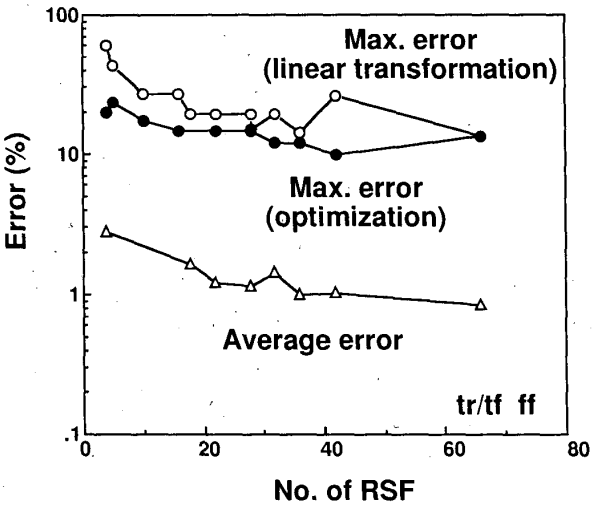


Fig. 6 Maximum and average errors in RSF with proper transformation

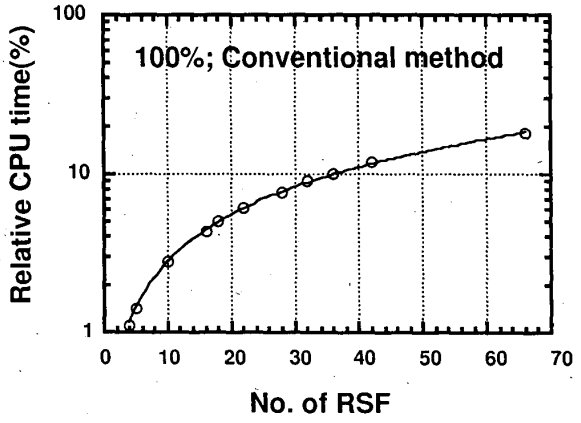


Fig. 7 CPU time dependence on number of RSF