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Engineering Systematic Yield of Fully-Depleted SOI MOSFET

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Abstract - we propose a new and effective SOI yield engineering methodology by sophisticated usage of 2D simulations. It is revealed by the methodology that, applying a limitation to threshold voltage yield and considering varied SOI layer thickness, the maximum current becomes substantially low. This trade-off relationship is balanced to obtain high maximum current and moderate source-drain breakdown voltage in acceptable turn around time.

I. Introduction

SOI is a promising technology for low-voltage applications. Especially, fully-depleted(FD) SOI MOSFET has advantages in short channel effects and subthreshold characteristics[1]. Process design for systematic yield of FD SOI MOSFETs requires specific consideration on floating-body effects and parasitic channel leakage currents. The influence of varied SOI layer thickness(σT_{soi}) to such phenomena is also complicated and substantial. So it is difficult to design SOI devices via experiments alone, and it is consequently important to optimize process sequences with TCAD for shorter development cycles and lower fabrication costs. The practical use of TCAD for SOI process, however, may not be easy. Subthreshold hump characteristics are pure 3D effects. Also LOCOS simulation on buried oxide is a demanding task. In this paper, we propose a new and effective SOI yield engineering methodology by sophisticated usage of 2D simulations. It is revealed by the methodology that, applying a limitation to threshold voltage(Vth) yield and considering σT_{soi}, the maximum current(Ids) becomes substantially low. This trade-off relationship is balanced to obtain high Ids and moderate source-drain breakdown voltage(BVsd) in acceptable turn around time.

II. Process architecture

Fig.1 shows cross sections of FD SOI nMOSFET. We focus on floating-body and LOCOS isolation type. An active edge BF_2 implantation(AE Impl.) is adopted near LOCOS edge to reduce subthreshold hump characteristics. LOCOS thickness(T_{locos}) and oxide thickness of LOCOS edge(T_{edge}) are determined by oxidation and etching conditions. Lateral electric field is reduced by LDD As implantation.

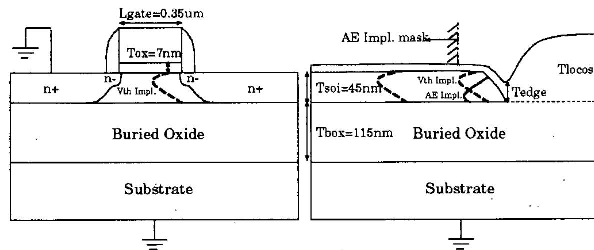

Fig. 1: Cross sections of FD SOI nMOSFET. An active edge BF_2 implantation adopted near LOCOS edge. T_{locos} and T_{edge} is determined by oxidation and etching conditions.

III. Methodology

Without using time-consuming 3D simulators, we use only 2D process and device simulators even to simulate 3D effects such as parasitic channel leakage. In this case surface carrier concentration along the channel width direction is simulated, and subthreshold current is calculated by multiplying appropriate mobility to the total surface carrier concentration(Fig.2).

Field LOCOS oxide shape is successfully simulated even after growing oxide reaches buried oxide, and after field oxide is slightly etched off during the removal of buffer oxide.

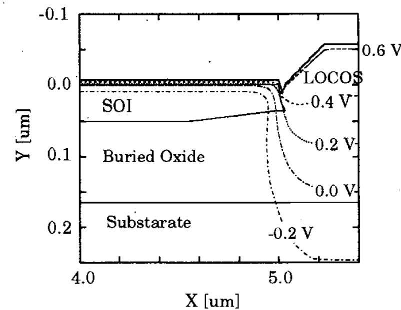

Fig. 2: Potential distribution in LOCOS edge considering SOI thinning by lateral oxidation. Simulation for IdVg hump requires accurate prediction topologically.

And for BVsd, non-local impact ionization model[2] is necessary to predict the floating-body effect accurately. We use process/device simulator OPUS/ ODESA[3] for these simulations. For parameter optimization, response surface function(RSF) are extracted from simulations according to design of experiments (DOE) [4]. Statistical information is calculated by Monte Carlo method using these RSFs. The statistical information is again converted to RSF and used in process optimization [5]. Our methodology for engineering yield of FD SOI MOSFET consists of following 4 steps(Fig.3).

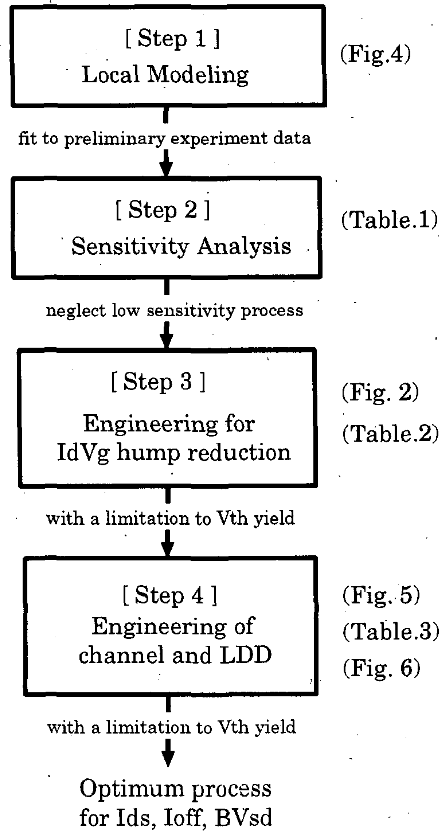

Fig. 3: Flow-chart of SOI yield engineering methodology based on 2D simulators

step1: Local Modeling: Before process engineering, it is important to adjust the model parameters to preliminary experiment data (Local Modeling). Fig.4 shows that predicted results by 2D simulation agree with experimental data of subthreshold hump characteristics.

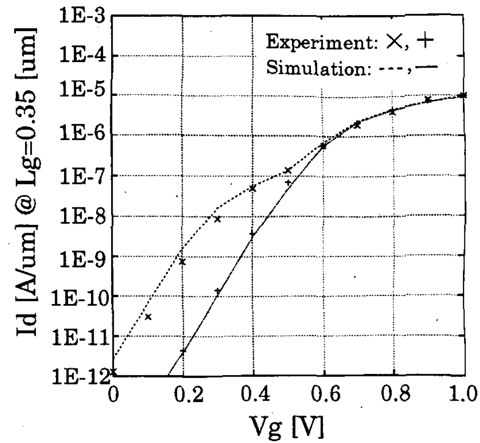

Fig. 4: Local modeling results. Predicted results by 2D simulation are well fitted to experimental data of IdVg hump characteristics.

step2: Process sensitivity analysis and RSF construction: Table.1 illustrates the device performance trends of SOI processes by sensitivity analysis. Sensitivity of buried oxide thickness(T_{box}) is negligible but T_{soi} is one of the main factors to design device performances in this architecture. Before further optimization, RSFs on many process parameters are constructed by number of DOE simulations. In our methodology, each simulation need only 20 CPU minutes including all characteristics for one device. Half a day is sufficient for all simulations.

Table 1: Illustration of device performances trend increased each process parameter. Sensitivity of Tbox is negligible. Tsoi is one of main factors to design device performances in FD SOI MOSFETs.

	Tsoi	Tbox	Vth dose	LDD dose	LDD energy	Tedge	AE dose
Vth	↗	→	↗	→	→	→	→
σ Vth	↘	→	↗	→	→	↘	↘
Ids	↘	→	↘	↗	→	→	→
σ Ids	→	→	↘	↗	→	→	→
Ioff	↘	→	↘	→	↗	↘	↘
BVsd	↗	→	↘	↗	↘	→	→
E// max	↘	→	→	↘	→	→	→

step3: Engineering for subthreshold hump reduction: Process engineering for reducing parasitic channel leakage is important. Target response of the optimization is Vth, Vth variation(σVth) and subthreshold swing(S-factor) as hump criteria. Subthreshold hump characteristics are effectively reduced by LOCOS edge oxide thickness(T_{edge}) and dosage of AE implantation (Table.2).

Table 2: Optimization for hump reduction with a limitation of Vth yield. Tedge and active edge implantation are effective to reduce hump characteristics. Because of hump reduction, σ Vth is also reduced.

	Spec. limits	Before optimization	Optimum for hump
Tedge [nm]	8 - 12	8.0	12.0
Active Edge Implantation dosage [/cm2]	0 -1E12	Not Implanted	1E12
Active Edge Implantation energy [keV]	60 - 70	Not Implanted	60
Sfac. [mV/dec] (Hump Criteria)	< 70	186.5	68.9
Vth	0.50 -0.60	0.545	0.572
3σ Vth	minimize	39.5	18.9

step4: Engineering of channel and LDD: Engineering the channel and LDD profile is necessary for BVsd and off-state leakage current(Ioff), which are often critical on SOI MOSFETs. In the limitations of Vth and Ioff, BVsd target is expected to be as high as possible. From information of fabrication process, 3 percent of L_{gate}, gate oxide thickness(T_{ox}) and T_{soi} are considered as 1σ process variations. Fig.5 shows a trade-off relationship of BVsd and Ioff, this trade-off is optimized by Vth and LDD implantations.

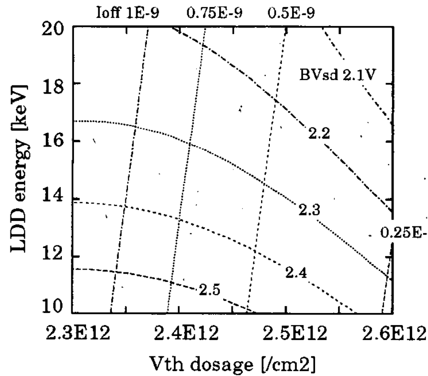

Fig. 5: Trade-off relationship of Ioff and BVsd. Process window exists Vth and LDD implantation parameters.

Table.3 shows results of optimization neglecting σT_{soi} (case A), considering σT_{soi} (case B) and considering σT_{soi} with maximizing Ids preferentially (case C). Applying to Vth limitation and considering σT_{soi} (case B), Ids becomes substantially low compared with case A as results of BVsd and Ioff limitations. In case C, this trade-off relationship is efficiently balanced by weighted optimization. Fig.6.

Table 3: Optimization of channel and LDD with a limitation of Vth yield. Case.A: σT_{soi} effect is neglected, Case.B: σT_{soi} is considered, Case.C: σT_{soi} effect is considered and Ids maximize preferentially. Trade-off of Ioff and Ids is also important to determine the optimum. Simulation number is 77set and CPU time is 20min. in each set.

	Spec limits	Before Optimization	case A	case B	case C
Vth dosage [/cm2]	2.0 -2.6E12	2.3E12	2.0E12	2.4E12	2.0E12
LDD dosage [/cm2]	1.0 -3.0E13	2.0E13	2.4E13	1.5E13	1.5E13
LDD energy [keV]	10 -30	20	24	20	15
Vth [V]	0.45 - 0.65	0.572	0.496	0.587	0.502
3σ Vth [mV]	minimize	55.2	46.0	55.2	47.7
Ids [uA/um]	maximize	127.4	151.5	119.1	137.8
3σ Ids [uA/um]	minimize	23.5	25.5	22.8	23.0
Ioff [uA/um]	< 1E-8	1.5E-9	7.2E-9	1.1E-9	6.8E-9
BVsd [V]	maximize	2.1	2.1	2.2	2.1
E// max [V/cm]	minimize	3.1E5	3.0E5	2.9E5	3.2E5

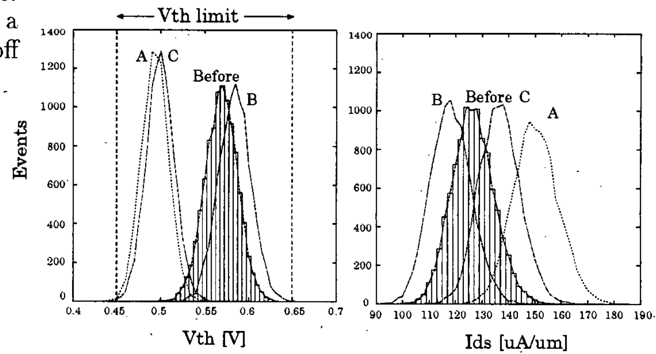

Fig. 6: Distribution of Vth and Ids applying Vth yield limitation. Applying to Vth limitation, σ Tsoi reduce Ids (comparison Case.A and Case.B), Finally Case.C minimize this trade-off by maximizing Ids preferentially.

IV. Conclusion

We presented a new methodology for engineering systematic yield of FD SOI MOSFET. Remarkable results are,

1) FD SOI process are effectively engineered by sophisticated usage of 2D simulators in acceptable turn around time.

2) After subthreshold hump characteristics is reduced by T_{edge} and active edge implantation, BVsd and Ioff are optimized by Vth and LDD implantations.

3) Applying a limitation to Vth yield and considering σT_{soi}, Ids becomes substantially low as results of BVsd and Ioff limitations.

4) This trade-off relationship is balanced to obtain high Ids and moderate BVsd by Ids weighted optimization.

References

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