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Advanced Process/Device Modeling and Its Impact on the CMOS Design Solution

Shigetaka KUMASHIRO

ULSI Device Development Lab., NEC Corporation
1120 Shimokuzawa, Sagamihara Kanagawa 229-1198, JAPAN

1. Introduction

Accurate global modeling is a key issue for the successful application of TCAD to the ULSI device design solution. To demonstrate how far we can go with the state-of-the-art global modeling, we tried to design 0.13 [μm] CMOS device by using our globally calibrated advanced process/device models. This paper reports the design methodology and the results compared with the fabricated device characteristics.

2. Process / Device Models

For the global process modeling, over 700 SIMS profiles were measured. Parameters for the dual-Pearson type Ion Implantation (I/I) model were extracted in the energy range from sub-keV to MeV[1]. The lateral scattering was evaluated by using the calibrated crystal-mode Monte Carlo (MC) I/I simulation[2]. Parameters for the boron (B), phosphorus (P), arsenic (As) and point-defect pair diffusion model[3] were determined according to the procedure described in [4]. Fig. 1 compares the profiles of the ultra shallow S/D-extension between the measurement and the simulation. It is shown that the simulation can reproduce the measurement with good accuracy except for the dopant out-diffusion from the surface. As for the device modeling, a standard drift-diffusion type device simulator was used in this work. Quantum mechanical correction was performed according to the result of the one-dimensional Schrödinger-Poisson solver whose example is shown in Fig. 2[5]. For the global device modeling, the MOS surface mobility model including the vertical field dependent Coulomb screening effect[6] has also been developed as shown in Fig. 3. In addition to accurate physical models, mesh quality is quite important to perform successful simulation. Mesh generation method using the "boundary protection layer" has been developed and applied both to device[7] and to process[8] simulators.

3. CMOS Design Methodology

Since the junction depth (Xj) of the S/D-extension is the most dominant factor for the short channel effect in the 0.13 [μm] CMOS device, the state-of-the-art technology of forming the shallowest junction profiles as shown in Fig. 1 was adopted as design premise. The gate oxide thickness and the threshold voltage (Vt) were determined by taking the constraints between the power supply voltage, the drive current (Idrive) and the off leak current into account. Then, the TCAD was used to determine the optimum channel and pocket I/I conditions that achieve the target Vt at the target minimum gate length (Lmin) of 0.12 [μm]. The Lmin was defined as the gate length (Lg) where the slope of the Vt-Lg characteristics becomes a predetermined value. To intuitively grasp the available design window and also to easily estimate the effect of the process fluctuation, several design maps were constructed. For example, Figs. 4 and 5 are the Lmin design maps of pMOS for the channel As I/I conditions and the tilted pocket As I/I conditions, respectively. According to the global modeling policy, all the simulations were performed without any local parameter adjustment.

4. Results

In Fig. 6, the single side gate-S/D overlap length (ΔL) and the S/D series resistance (Rsd) evaluated by using the Modified-Shift-and-Ratio method[9] are compared between the fabricated devices and the simulation. As shown in Fig. 6 (a), the simulation shows a reasonable predictability for As in the nMOS.

On the other hand, the simulation significantly overestimates the ΔL of B in the pMOS as shown in Fig. 6 (b). Since the difference in the ΔL is much larger than that in the Xj shown in Fig. 1 (b), this is probably due to the unconsidered effect in the two-dimensional B diffusion. Fig. 7 compares the electrical characteristics of the devices fabricated without pocket I/I. The Vt-Lg characteristics show reasonable agreement as shown in Fig. 7 (a). Moreover, even the drift-diffusion type device simulator can predict the Idrive-Lg characteristics with good accuracy as shown in Fig. 7 (b). Fig. 8 shows the Vt-Lg characteristics of the devices fabricated with the tilted pocket I/I. The simulated results are not so accurate as those of the devices without pocket I/I. This is probably due to the combination of the following three effects. First, the channeling in the MC I/I model was inaccurate. Second, the lateral diffusion of S/D-extension was excessive. Third, non-uniform quantum mechanical correction was necessary in the pocket region.

5. Conclusion

It has been demonstrated that the TCAD with the state-of-the-art global modeling can be applicable to the 0.13 [μm] CMOS design in terms of the prediction of the S/D-extension junction depth, the channel profile and the drive current. Further model improvement is required for more accurate prediction of the ΔL and the Vt-Lg characteristics of the devices with the tilted pocket I/I.

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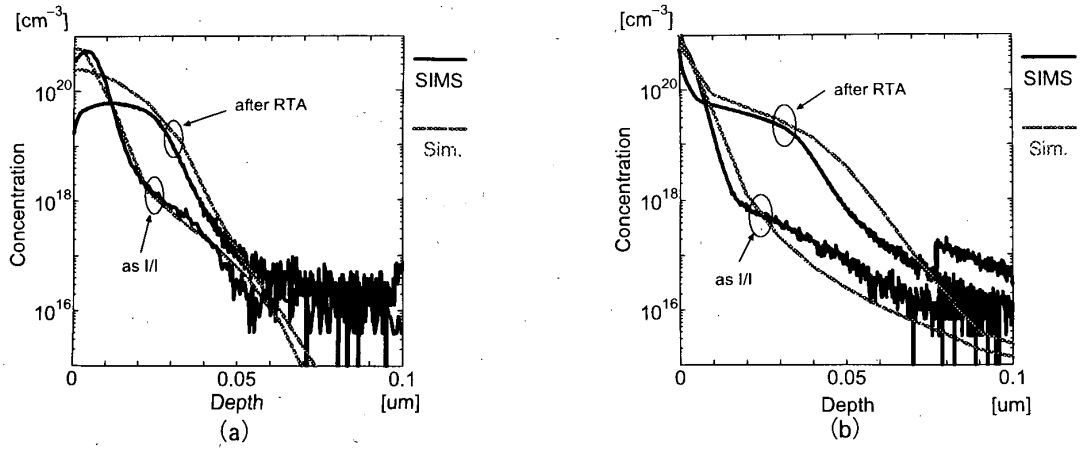

Fig.1 B, P, As and point-defect pair diffusion model with a unified parameter set can reproduce the ultra shallow S/D-extension profiles except for the out-diffusion from the surface. (a)As for nMOS. (b) B for pMOS.

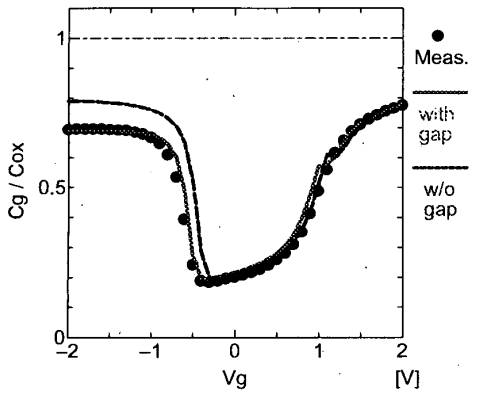

Fig. 2 Calculation example of quantum mechanical model. By inserting the low concentration thin gap layer at the interface between poly-Si and gate oxide, the measured full Cg-Vg characteristics can be reproduced.

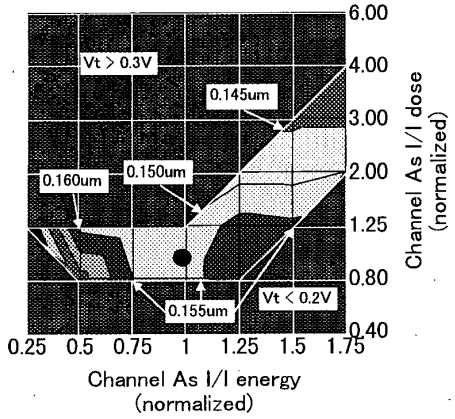

Fig. 4 Lmin vs pMOS channel As I/I condition map calculated by using TCAD. The circle is an adopted design point.

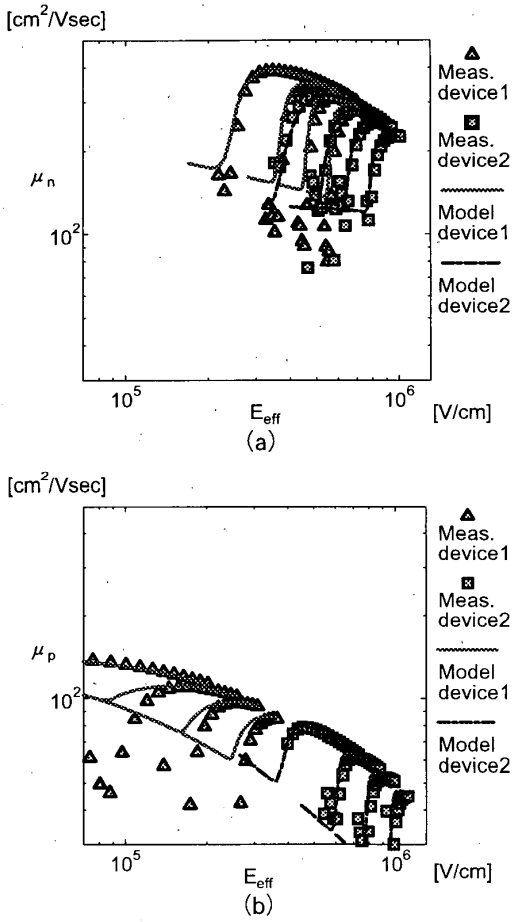

Fig. 3 MOS surface mobility model including the vertical field dependent Coulomb screening effect can reproduce the measurement both in the roll-off and the universality regions. (a) electron mobility. (b) hole mobility.

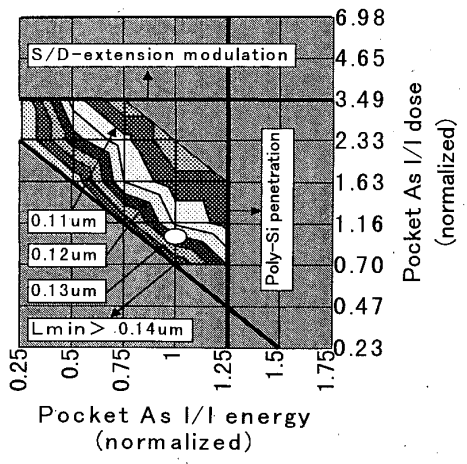

Fig. 5 Lmin vs pMOS tilted pocket As I/I condition map. The circle is an adopted design point.

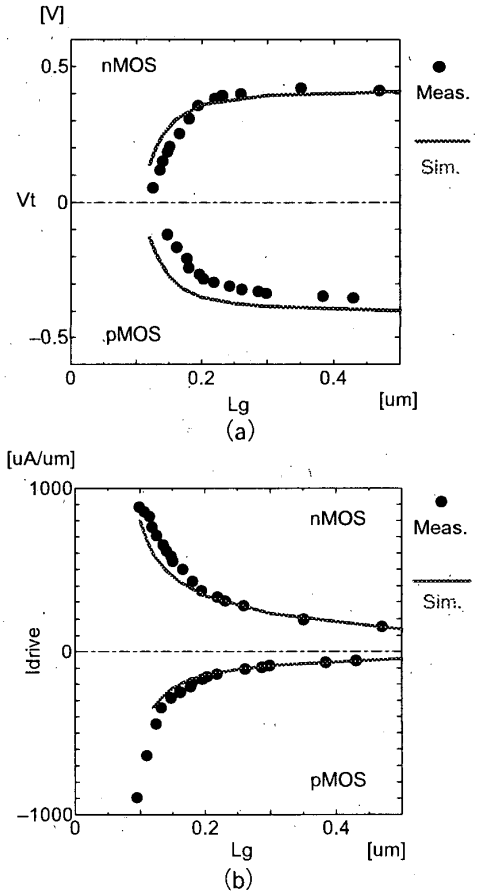

Fig.7 Comparison of the (a) Vt-Lg and the (b) Idrive-Lg characteristics between the measurement and the simulation for the CMOS fabricated without pocket I/I. Vt shows reasonable agreement. Even a drift-difusion type device simulator can predict Idrive with good accuracy.

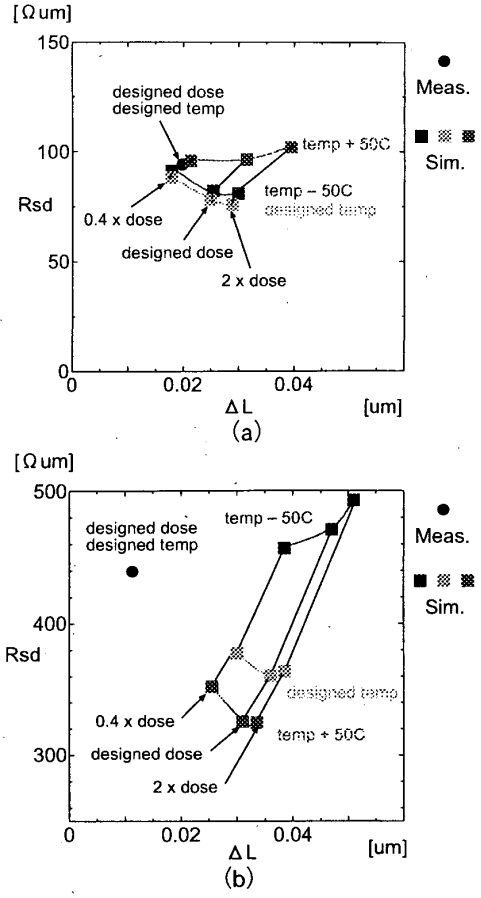

Fig.6 Comparison of the ΔL-Rsd characteristics between the measurement and the simulation. (a) The simulation shows a reasonable predictablity for nMOS. (b) The simulation significantly overestimates ΔL in pMOS.

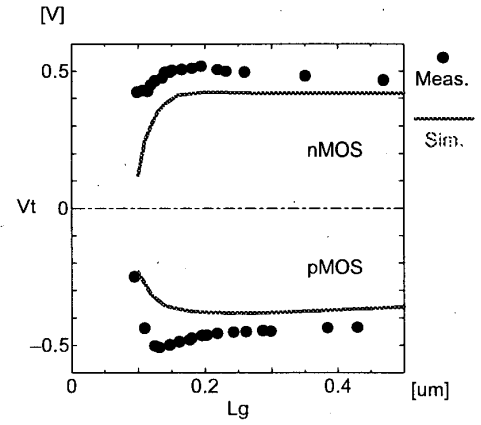

Fig. 8 Comparison of the Vt-Lg characteristics for the CMOS with pocket I/I. Further model improvement is required for more accurate prediction.