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Sub-0.1 μm Device Simulation Technology: Another Problems for Monte Carlo Simulations

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abstract

A brief overview of unsolved issues for sub-0.1 μm Si-MOSFETs that are appropriate to be tackled by the Monte Carlo method is presented. Also, our recent results of the Monte Carlo studies on the dynamical and intrinsic current fluctuations in Si-MOSFETs are presented. It is demonstrated that, as the number of the channel electrons decreases, the normalized standard deviation of the current variance attains a significant fraction of the averaged drain current when the device width is reduced into deep sub-μm. It is also shown that this current fluctuation mainly results from the thermal noise in the heavily-doped source and drain regions and, consequently, is nearly independent of the supply drain voltage.

1 Introduction

With the successful analyses of ultra-small Si-MOSFETs via Full-Band Monte Carlo (FBMC) simulations,[1] it is conjectured that many problems associated with Monte Carlo (MC) method were settled down. In addition, because of the reduction of the supply voltage, it was hoped that hot-electron degradation effects, of which the Monte Carlo simulation is most powerful for the analyses, would be significantly reduced. It is our purpose of this paper to show that these conjectures are somewhat too optimistic and there are still many issues that should be tackled by the MC method.

In the present paper, we shall give a brief overview of the issues left to be attacked by the MC method, and our recent MC studies on the (dynamical and intrinsic) current fluctuations in Si-MOSFETs, which have so far received very little attention, on the contrary to the static fluctuation issues such as the threshold variation due to dopant fluctuations.[2, 3]

2 Another Problems for Monte Carlo Simulations

2.1 Long-range Coulomb interaction

According to the recent study,[4] as devices are scaled down further, the long-range Coulomb interaction between the electrons greatly enhance the high-energy tail of the electron energy in the channel. The mutual Coulomb interactions among electrons in the heavily-doped source and drain contacts result in an extra component of the kinetic energy of electrons and give rise to nonthermal high-energy tails of the energy distribution. For small devices, this is penetrated into the significant fraction of the channel and there exists an anomalous high-energy tail in the channel electrons that becomes a dominant cause of the hot-electron degradation. This implies that the hot-carrier issues could be still significant under the reduced supply voltage and the FBMC method ought to be employed to solve the problems.

2.2 Fluctuation issues of device characteristics

The device-property fluctuations have received a great attention recently because of the shrinkage of the device size. Threshold voltage variation due to dopant fluctuations is, among others, a typical example of such fluctuation issues.[5, 6, 7, 8, 9, 10] These problems are usually studied with the 2-D or 3-D drift-diffusion-type simulators.[9, 10] The threshold shift results in the variation of the number and the position of impurities. These give rise to the variation of the electric potential in the depletion layer and strongly affects the electron path. In order to take account of the locality of impurities, the 'atomistic' approach, in which a fine grain discretization of the mesh is employed to solve the 3-D Poisson equation, is porposed.[9] Probably, this is the best approach we could take at present, yet far more distant to be satisfactory: Since the threshold shift results in the variation of the electron path in the SiO_2/Si interface, the MC method would be appropriate to evaluate the correct electron path under the Coulomb interactions in the channel adjacent to heavily-doped source and drain contacts. Nevertheless, the treatment of the atomistic and short-range nature of the Coulomb interaction between the electron and the localized impurity is not a trivial problem.[11]

In addition to the static fluctuation issues like the threshold variation, the (time-dependent) dynamical fluctuation of device properties such as the drain current variance could be of great importance as the reduction of *entire* device size proceeds.[2, 3] As the device width W is scaled down into the deep sub-μm regime, the number of electrons in the channel drastically decreases and the fluctuation in number of the channel electrons, which is manifested by the central limit theorem,[12] can be no longer ignored. As a result, the miniaturization of the device width W introduces the time-dependent current fluctuation. It should be noticed that this current fluctuation results from the graininess of electrons in the channel and is intrinsic in the sense that it cannot be removed in principle. In the followings, our MC simulation results of the above-mentioned current fluctuation are discussed.

3 Dynamical Fluctuation: Intrinsic Current Fluctuation

3.1 Monte Carlo simulation method

The present analyses of the current fluctuations are carried out under a typical Si-MOSFET structure with the effective channel length $L_{\rm eff}$ = 300 and 40 nm. Simulations are performed by using the ensemble Monte Carlo method under the fixed potential profile obtained from the conventional 2-D Drift-Diffusion simulator. The Monte Carlo method employed here is a simple and conventional one; the analytical (nonparabolic) electronic band structure and the material parameters for Si known in the literature are used.[13] The periodic boundary condition is assumed at the source and drain contacts so that the number of all simulating electrons inside the device does not change. The number of simulating electrons is determined by the device width W *provided that each simulating electron corresponds to a real electron.* Electron kinetics is simulated for several ten ps and the device characteristics, such as the current and current variance, are sampled after a transient of 5 ps. The channel current $I(t)$ at time t is evaluated using the Ramo-Shockley formula[14] and recorded at every 1 fs.

3.2 Significance of current fluctuation

A typical drain voltage dependence of the drain current $I_{\rm ave}$ and the variance (fluctuation) of the drain current $\langle \delta I^2 \rangle$ is shown in Fig 1 (a). Notice that the current variance is almost independent of the drain voltage. As shown in the next subsection, this is due to the fact that the current fluctuation is dominated by the (quasi-equilibrium) thermal noise in the heavily-doped source and drain regions adjacent to the channel and, thus, independent of the supply voltage. Significance of the current fluctuation for small devices with the reduced width W can be clearly seen in Fig. 1 (b), in which the time series of the drain current obtained from the MC simulations for Si-MOSFET with $L_{\rm eff}$ =300 nm and W =150 nm are shown. Notice that the fluctuation often exceeds a significant fraction of the averaged drain current ($I_{\rm ave} \approx$ 15 μA).

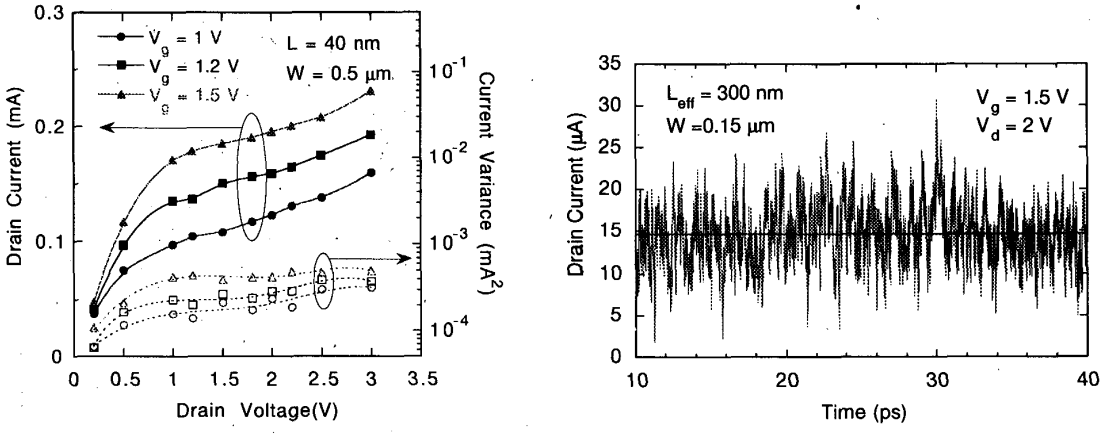

Figure 1: (a) Typical drain voltage dependence of the drain current (left scale) and the variance of the drain current (right scale) $\langle \delta I^2 \rangle$, obtained from the MC simulations for the n-channel Si-MOSFET with $L_{\rm eff}$ =40 nm and W =500 nm. (b) Time series of the drain current in the n-channel Si-MOSFET with $L_{\rm eff}$ =300 nm and W =150 nm.

Under the quasi-equilibrium situations, the thermal noise is essentially equivalent to the shot noise.[15] Therefore, the current variance $\langle \delta I^2 \rangle$ may be approximated by the Shottky formula for the shot noise: $\langle \delta I^2 \rangle = 2q\, I_{\rm ave}\, \Delta f$, where Δf is the frequency band width. Since the averaged drain current is approximately propor-

tional to the device width W, the normalized standard deviation of the drain current becomes

$$\frac{\langle \delta I^2 \rangle}{I_{\rm ave}} = \sqrt{\frac{2\,q\,\Delta f}{I_{ave}}} \propto \frac{1}{\sqrt{W}} \quad . \tag{1}$$

Therefore, the reduction of the device width W leads the decrease of the number of the channel electrons and the enhancement of the normalized standard deviation of the current. It should be noted that Eq. (1) is essentially equivalent to the central limit theorem from the probability theory. The normalized standard deviation of the drain current $\langle \delta I^2 \rangle / I_{\rm ave}$ for various device widths W obtained from MC simulations is plotted in Fig. 2. The standard deviation indeed increases as the device width is reduced and is well approximated by Eq. (1). We would like to stress that deviation attains even several ten % when the device width is scaled down into deep sub-μm.

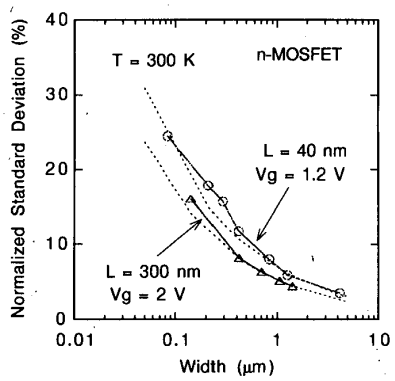

Figure 2: Normalized standard deviation of the drain current $\langle \delta I^2 \rangle / I_{\rm ave}$ as a function of the device width W of Si-MOSFETs with the channel length of $L_{\rm eff}$ =40 and 300 nm. The dotted line is the prediction described in the text; $\langle \delta I^2 \rangle / I_{\rm ave} \propto W^{-1/2}$.

3.3 Spatial origin of current fluctuation

The intrinsic current fluctuation becomes a significant fraction of the averaged drain current when the device width is scaled down. As mentioned in the previous subsection, this current fluctuation originates from the thermal noise in the heavily-doped source and drain regions. This can be shown by investigating the spatial dependence of the current variance (fluctuation), as follows. Under the assumption that the electron inside the device does not correlate each other, the current variance $\langle \delta I^2 \rangle$ can be approximated as

$$\langle \delta I^2 \rangle = \left(\frac{q}{L}\right)^2 \langle \sum_{i=1}^{N} \sum_{j=1}^{N} \delta v_i \, \delta v_j \rangle \approx \left(\frac{q}{L}\right)^2 \langle \sum_{i=1}^{N} \delta {v_i}^2 \rangle \quad . \tag{2}$$

Here, q, L, N, and v_i are the magnitude of electronic charge, the device length, the total number of electrons and the *i-th* electron velocity-deviation along the channel direction, respectively. Notice that the number N of all electrons inside the device is fixed in the present MC simulations and, thus, the current variance entirely results from electron's velocity variance; the current variance is the sum of the velocity variance of each electron in the device. Therefore, the spatial origin of the current variance is found by locally summing the velocity variance of each electron at various positions inside the device.

The results thus obtained are shown in Fig. 3, where the local current variance ${\sigma_{loc}}^2$ is plotted for Si-MOSFETs with $L_{\rm eff}$ =300 and 40 nm. As for Si-MOSFET with $L_{\rm eff}$ =300 nm, the local current variance ${\sigma_{loc}}^2$ has large values in the heavily-doped source and drain regions, compared with the magnitude of ${\sigma_{loc}}^2$ in the channel. This is simply because ${\sigma_{loc}}^2$ depends on the number of electrons residing in that region. Also, ${\sigma_{loc}}^2$ is almost independent of the supply drain voltage, which is a remarkable contrast to the cases of bulk or/and 1-D *nin* structures.[2] Hence, the current variance under Si-MOSFET structures is nearly independent of the supply drain voltage and the (quasi-equilibrium) thermal noise in the source and drain regions dominates the *entire* current variance.

The situation is slightly different for the case of Si-MOSFET with $L_{\rm eff}$ =40 nm. The overall features of the current variance is similar to those of Si-MOSFET with $L_{\rm eff}$ =300 nm, but the fraction of ${\sigma_{loc}}^2$ in the channel and drain regions variance is more enhanced with respect to the *entire* current variance. In addition, the drain-voltage dependence appears, though it is still weak. Thsese results are intimately related to the *hot-drain*

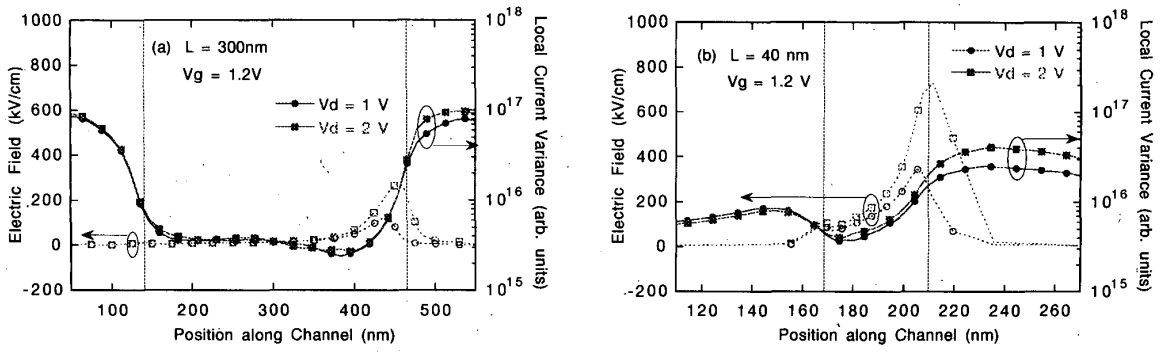

Figure 3: Local current variances $\sigma_{loc}{}^2$ as a function of the position along the channel for Si-MOSFETs with (a) $L_{\rm eff}$ =40 nm and (b) $L_{\rm eff}$ = 300 nm.

resulted from the quasi-ballistic electrons in such ultra-small devices. Since the electrons quasi-ballistically transport in ultra-small devices, the drain regions adjacent to the channel are heated by high-energy electrons injected quasi-ballistically from the channel. Furthermore, such high-energy electrons in the drain edge, after suffering scatterings, could be kick-backed into the channel.[3] These make the drain and the channel regions hotter, and the velocity variance in the channel and drain regions is increased.

4 Summary

A brief overview of unsolved issues for sub-0.1 μm Si-MOSFETs that are appropriate to be solved by the Monte Carlo method has been given. Our recent studies of the intrinsic current fluctuation with the Monte Carlo simulation under Si-MOSFET structures has been presented. It has been demonstrated that the normalized standard deviation of the current variance reach a significant fraction of the averaged drain current when the device width is reduced into deep sub-μm. It has been shown that this current fluctuation mainly results from the thermal noise in the heavily-doped source and drain regions and, consequently, is nearly independent of the supply drain voltage.

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