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A Compact Lateral-SOI BJT Model for RF Circuit Simulation

Tsuneaki Fuse, *Shigeru Kawanaka, **Kazumi Inoh, and *Tomoaki Shino

Computer & Network Laboratory, Toshiba Corporation
*Advanced LSI Technology Laboratory, Toshiba Corporation,
**Microelectronics Engineering Laboratory, Toshiba Corporation,
1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki 210-8582, Japan
TEL:044-549-2232, FAX:044-520-1841, E-MAIL:tsuneaki.fuse@toshiba.co.jp

1. INTRODUCTION

Lateral bipolar transistors using SOI technology (lateral-SOI BJTs) are promising for low-power RF chips in portable communications equipment, owing to their inherently small parasitics[1][2]. In high-frequency region above 1GHz, however, the unique device structure degrades the accuracy of the circuit simulation using the MGP model. This paper describes a compact equivalent circuit model for lateral-SOI BJTs, in which parasitic effects depending on the device structure are taken into account precisely, based on results of 3-dimensional device simulation.

2. CONCEPT OF PROPOSED MODEL

The lateral-SOI BJT, a simple device structure without any parasitic pn-junction, requires comparatively large contact regions for connecting to base, emitter, and collector terminals, as shown in Fig.1. These contact regions are coupled to the silicon substrate through the buried oxide. The coupling effects on high-frequency characteristics were analyzed in detail by using 3-dimensional device simulator. In the common-emitter configuration, the emitter-to-substrate capacitor, Ces, had no effect on the small-signal characteristics, but the base-to-substrate capacitor, Cbs, and the collector-to-substrate capacitor, Ccs1, had effects mainly on the input admittance, y11, and the output admittance, y22, respectively.

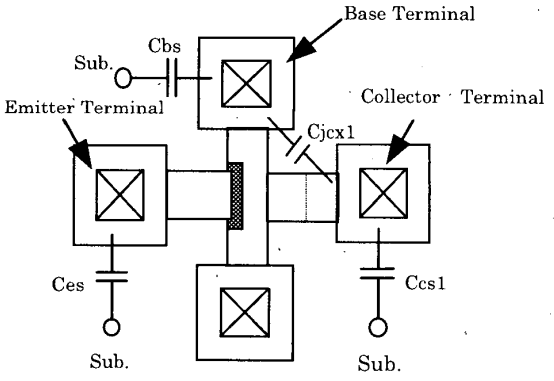


Fig.1 Top View of Lateral-SOI BJT

Figure 2 shows the proposed equivalent circuit for the lateral-SOI BJT. In this model, three terminal-to-substrate capacitors mentioned above and an external base-to-collector terminal capacitor, Cjcx1, are introduced. Furthermore, the internal collector-to-substrate capacitor, Ccs, is

removed from the conventional MGP model. In the lateral-SOI BJT, the value of emitter resistance, Re, is less than 10% of that of the base resistance, Rb. Assuming that the emitter resistance is negligibly small, y-parameter of the proposed equivalent circuit can be simply described as follows.

$$y11 = y11(MGP) + j\omega(Cjcx1 + Cbs) \quad (1)$$

$$y12 = y12(MGP) - j\omega Cjcx1 \quad (2)$$

$$y21 = y21(MGP) - j\omega Cjcx1 \quad (3)$$

$$y22 = y22(MGP) + j\omega(Cjcx1 + Ccs1) \quad (4)$$

where yij(MGP) represents y-parameter obtained from the MGP model with Ccs=0 and Re=0 (i, j=1 or 2).

By using 3-dimensional device simulator, DC and small-signal analyses were performed to extract the SPICE parameter. Main parameters for the analyzed device are listed in Table 1. Eqs. (1)-(4) were then calculated under the given bias condition by applying the SPICE parameter to the equivalent circuit shown in Fig.2. It is noted that in our calculation the effect of excess phase does not take into consideration.

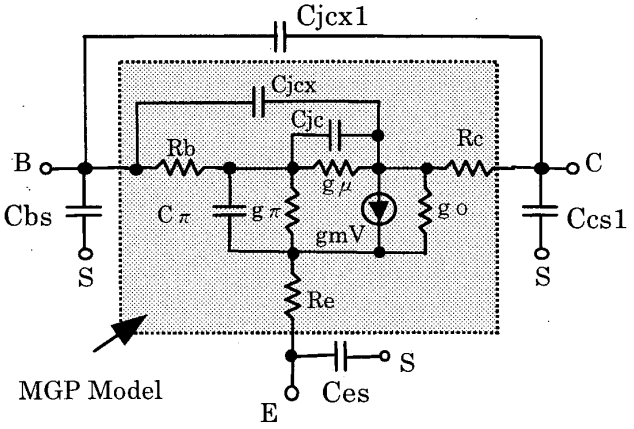
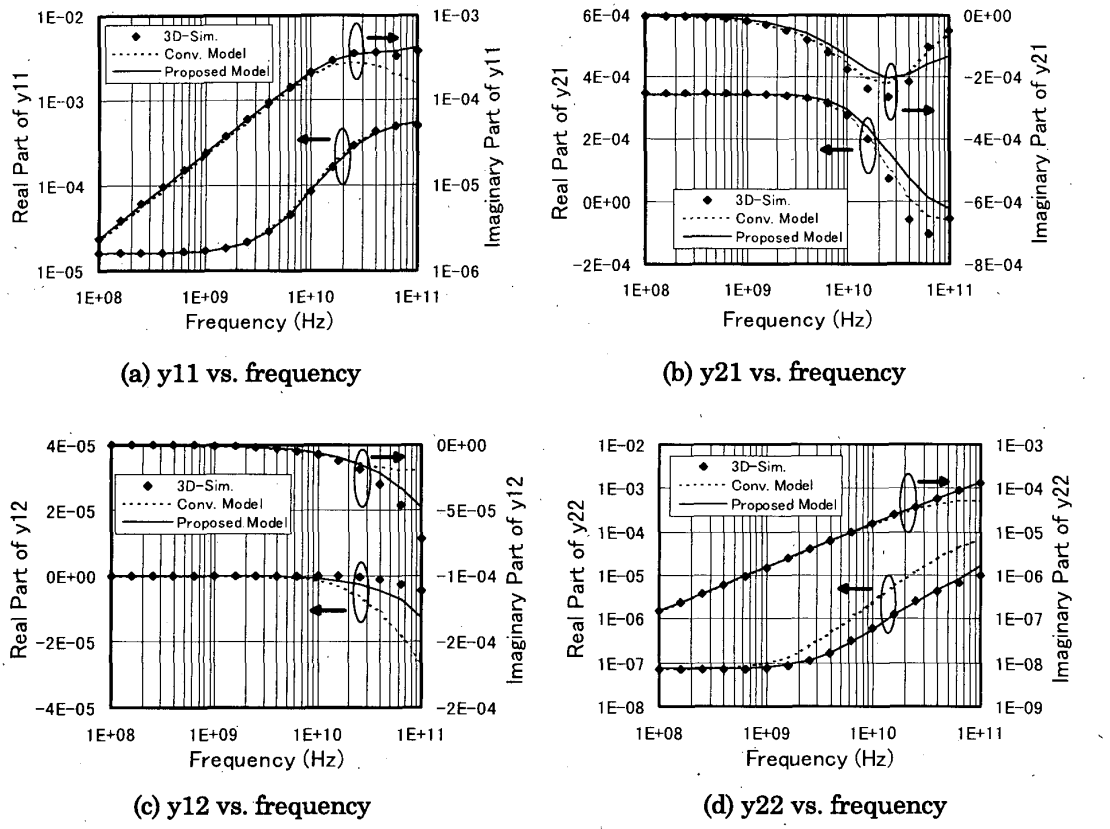


Fig.2 Equivalent circuit for lateral-SOI BJT.

Table 1 Main device parameters in 3D-device simulation.

Emitter width	0.3um
SOI thickness	0.15um
Cbs	0.4fF
Cjcx1	0.04fF
Ccs1	0.13fF

Figure 3 shows frequency response of y-parameter in the case of Vbe=0.875V and Vce=2.0V. It was shown that the conventional model (dashed-line) underestimated the imaginary part of y11 and overestimated the real part of y22. The deviation was large for high-frequency region above 1GHz. On the other hand, the proposed model (solid-line) improved the accuracy, due to additional terminal capacitors. The proposed model also improved the accuracy for y12, whereas some deviation was found in y21 between results of 3-dimensional device simulation and the proposed model. This is because y21 is a function of the small-signal transconductance, gm, which is modulated by excess phase [3]. By using SPICE simulation, it was confirmed that excess phase parameter (PTF) of 20 degree gave in good agreement with the result of 3-dimensional device simulation.



(a) y11 vs. frequency

(b) y21 vs. frequency

(c) y12 vs. frequency

(d) y22 vs. frequency

Fig.3 Comparison of y-parameter between 3D-simulation and calculation by Eqs.(1)-(4) (Vbe=0.875V, Vce=2.0V).

3. MODEL VERIFICATION

The maximum oscillation frequency, fMAX, one of the figures of merit determining RF performance, is defined as the frequency where either the maximum stable gain (MSG) or the maximum available gain (MAG) is unity. The overestimation in the real part of y22 is supposed to degrade the power-gain and fMAX. The proposed model was verified by S-parameter measurements for five samples with emitter size of 0.6um*0.1um. SPICE simulation was performed by using the sub-circuit, in which the additional terminal capacitors were introduced, corresponding to the proposed equivalent circuit.

Figure 4 shows the comparison of power-gain, MAG/MSG, between measurements and SPICE simulation. The base bias of 0.92V gives around the peak value in fMAX. Under this bias condition, the conventional model underestimated MAG by 1-2dB in the range of 1 to 10GHz. This is due to the overestimation in the real part of y22. As a result, the conventional model produced a maximum error of 33% in fMAX for average data of five samples, whereas accuracy was improved within 8% in the proposed model (Ic<1mA), as shown in Fig.5.

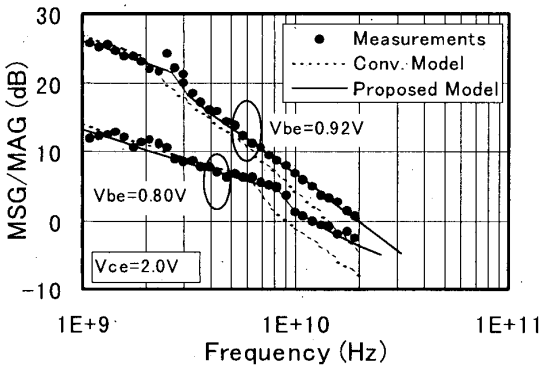


Fig.4 Comparison of power-gain between measurements and SPICE simulation.

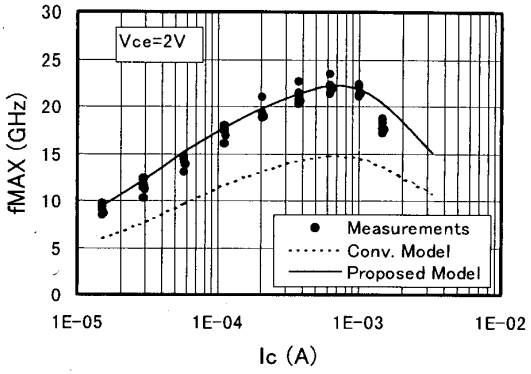


Fig.5 Model verification in fMAX-Ic characteristics.

4. CONCLUSION

By using 3-dimensional device simulator, parasitic effects around the contact region for a lateral-SOI BJT were analyzed in detail. It was shown that the parasitic terminal capacitors had effects mainly on the input and output admittance y11 and y22 in high-frequency region above 1GHz. Based on the analysis results, a compact model was proposed for circuit simulation, and maximum error within 8% was achieved in fMAX. This lateral-SOI BJT model is indispensable for realizing low-power and high frequency RF circuits.

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