Effects of scaling and lattice heating on n-MOSFET performance via electrothermal Monte Carlo simulation

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Abstract

The technological advances which have enabled fabrication of devices ever deeper into the submicron regime have left many new and unexplored theoretical questions in their wake. In this study, we investigate the effect of self-heating on charge transport and oxide degradation in n-channel MOSFETs as a function of channel length and applied bias via the Monte Carlo and hydrodynamic methods. We demonstrate the increasing importance of self-heating with decreasing device dimension, and show that even moderate lattice heating can significantly suppress the high energy tail of the electron distribution function as well as influence the oxide degradation rate under normal device operation.

1. Introduction

Electrothermal device simulation is often employed to investigate the operation of power devices and ESD protection circuits [1, 2], where enormous currents give rise to lattice temperatures in excess of 600K. In SOI MOSFETs, despite considerably lower current levels, a significant amount of self-heating [3, 4] results from the confined nature of the heat flow. We examine the extent to which a self-heating effect exists in conventional submicron n-MOSFETs, and discuss the ramifications on charge transport and oxide lifetime.

2. Model Description

We approximate the Bose-Einstein phonon distribution with a single lattice temperature applied to all 6 branches of the Si phonon spectrum, and solve the lattice heat equation with a temperature-dependent heat coefficient; device contacts serve as thermodes for the purpose of boundary conditions. Carrier-phonon scattering rates for the Monte Carlo simulator are pre-tabulated as a function of lattice temperature, and interpolated during the simulation based on particle position and the solution of the lattice heat equation. Self-consistency is achieved through feedback of the carrier-phonon energy loss rates to the driving terms of the heat equation.

We estimate oxide lifetime by means of an Eyring model, first proposed by McPherson and Baglee [5] to describe oxide breakdown in bipolar stress tests as a thermodynamic

process. The Eyring model has been subsequently reconfirmed over a wide range of ambient temperatures, oxide thicknesses and field strengths [6], where oxide trap generation is presumed to be the dominant damage mechanism. We expect the Eyring model to be valid above lattice temperatures of approximately 150K, below which a transition seems to occur to another mode of oxide degradation [7], namely channel hot carrier aging [8]. In the limiting case of $F \ll F_B$, where F_B is the instantaneous dielectric breakdown field, the Eyring model predicts an oxide lifetime of the following form:

$$\frac{1}{\tau_{BD}} = \tilde{C}(t_{ox})e^{-\frac{B_1(t_{ox})-B_2(t_{ox})F}{k_B T}}, \quad (1)$$

where $\tilde{C}$, B_1 and B_2 are, for a given nominal injection current, process-dependent functions of oxide thickness alone, which may be extracted from stress test data [6]. As stress test experiments are, for practical reasons, restricted to high fields, one must extrapolate the collected data with a properly parametrized Eyring formula in order to obtain estimates of oxide lifetime under realistic operating conditions.

3. Simulation and Analysis

In order to estimate the effect of device scaling on lattice temperature, we have performed a series of hydrodynamic simulations on n-MOSFETs of various channel lengths as a function of drain voltage. Our results, shown in Fig. a), demonstrate a marked rise in lattice temperature with decreasing channel length. Furthermore, the lattice temperature takes on a peaked, non-uniform distribution, as shown in Fig. b). At an ambient temperature of 300K however, the largest observed self-heating is on the order of 10% for an isolated transistor, and has negligible impact on the contact currents and electronic solution variables of the hydrodynamic equations.

Our Monte Carlo simulations indicate, however, a significant influence of self-heating on the high-energy tail of the electron distribution function, as demonstrated in Fig. c). At high energies, self-heating can suppress the electron distribution by orders of magnitude through nonlocal changes in the balance of energy gain and loss. This effect becomes even more pronounced in the case of EPROMs, where the higher bias levels lead to lattice temperatures exceeding 350K, as shown in Figs. d) and e). Our results indicate that the inclusion of self-heating effects can be critical to the proper modeling of gate current.

The point at which the lattice temperature takes on its peak value is dirrctly under the Si/SiO2 interface, just inside the LDD implantation region, corresponding to the point of maximum energy loss of electrons to phonons. An inevitable result of scaling is therefore an elevation of the average channel lattice temperature due not only to to the increase in peak lattice temperature, but also due to the proximity effect. This has consequences not only for the electron distribution function, as discussed above, but also for oxide lifetime. According to the Eyring model, elevated lattice temperatures in regions of high oxide field can result in a significant local reduction of oxide lifetime, even for modest self-heating at an ambient temperature of 300K. We demonstrate this effect in Fig. f), using the parameterization of [6]. To what extent the lattice temperature enhanced oxide degradation is offset under normal device operation by the reduction in gate current remains an open question.

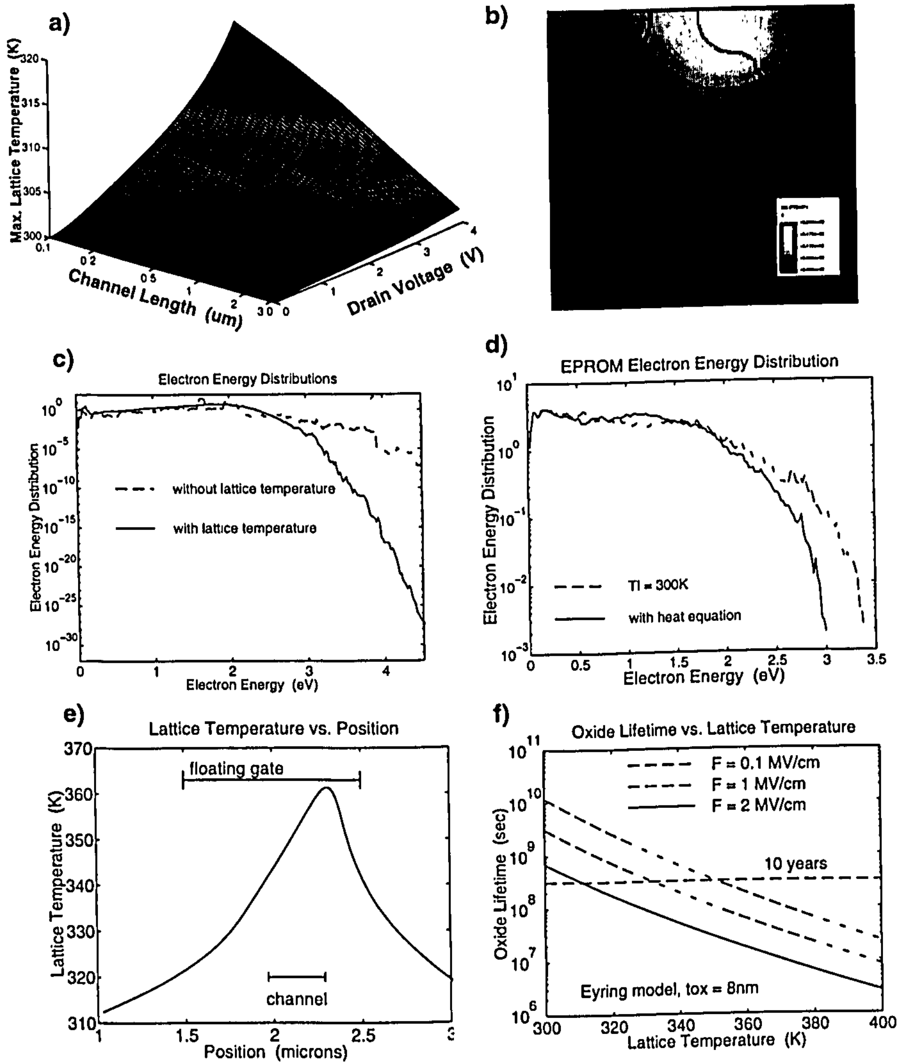

Figure 1
a) Self-heating as a consequence of n-MOSFET scaling. (hydro simulation)
b) Lattice temperature profile, Lg=0.1um, Vd=4V, Vg=2.3V. (MC simulation)
c) Elevated lattice temperature suppresses the high-energy electron distribution in MOSFETs.
d,e) High bias conditions in EPROMs lead to significant self-heating effects, affecting write times.
f) Theoretical sensitivity of oxide lifetime on lattice temperature, as predicted by the Eyring model with tox = 8 nm.

4. Conclusions

We have demonstrated that scaling of n-MOSFETs can result in self-heating which, although mostly negligible in its effect on the electronic solution variables of the hydrodynamic equations, can have a very significant impact on the high energy tail of the electron distribution function. Lattice heating is therefore a crucial factor for the proper modeling of gate currents in n-MOSFETs and EPROMs. Finally, by means of an Eyring model, we have shown that lattice heating during device operation may give rise to local changes in oxide lifetime, which may be the deciding factor in the lifetime of the device as a whole.

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